Development of high temperature diffusion barriers and a transient liquid-phase wafer bonding for thermoelectric MEMS energy harvester

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Abstract

In microsystem technology, a thermoelectric generator (TEG) can be fabricated in micro-scale structures (μTEG) using a surface silicon micromachining. In order to convert heat up to 600 °C into electrical power, a poly-SiGe semiconductor could be a suitable thermoelectric material. However, to the best of the author's knowledge, a development of a μTEG for these high temperature applications has not been published so far because, for such high temperature applications, the reliability and the stability of incorporating materials, *e.g.*, an electrical interconnection between poly-SiGe structures, can be challenging. The interconnection can be fabricated using a wafer bonding technique, where *p*-poly-SiGe legs on a wafer are bonded with *n*-poly-SiGe legs on the other wafer. This technique requires a bond solder, the components of which are deposited on a plating base. In respect to high temperature applications, the bond solder must not up to 600 °C heat melt and must remain conductive, and the plating base must have a high thermal stability, *i.e.*, prevents diffusion (diffusion barrier) into the semiconductor layer and must also remain conductive.

For this purpose, TiW-based and Ta-based diffusion barriers, which serve as the plating bases, and a Nickel-Tin Transient Liquid-Phase (Ni-Sn TLP) wafer bonding are developed. The TiW-based and Ta-based diffusion barriers are deposited in form of stacked thin films with a Ni top layer on 8"-wafers. In order to investigate the high thermal stability of both diffusion barriers, several methods; XRD analysis, TEM analysis (EDX and EFTEM analysis), SEM-EDX analysis, and 4-probe sheet resistance measurement, are performed before and after annealing. The annealing is performed in a vacuum chamber at given temperatures up to 600 °C for 24 h. After 600 °C annealing, no material diffusion into the Si substrate or poly-Si layer is determined. Both diffusion barriers exhibit a tolerable sheet resistance increase.

In the Ni-Sn TLP wafer bonding, Ni and Sn layers are subsequently electroplated on a 6"-waferpair using a self-made lab-scale electroplating tool and a pulsed electric current. This pulsed plating can enhance the thickness uniformity of Ni structures as well as the surface roughness of Sn structures. The plating bases are the TiW-based and Ta-based diffusion barriers with the Ni top layer. After wafer bonding, shear tests are performed on a number of selected dies to investigate the bond solder's mechanical strength and daisy chain dies are measured electrically to investigate the bond solder's electrical resistance. These investigations are performed on both types of bonded dies before and after annealing (in a vacuum ambient at 600 °C for 24 h). No re-melting of bond solder is observed after annealing. The Ni-Sn bond solder exhibits a relatively high bond strength before and after annealing, and the electrical resistance of a daisy chain structure exhibits a tolerable increase after annealing. The Ni-Sn phase of the bond solder before annealing transforms into a new stable phase after annealing. According to the Ni-Sn phase diagram, this new stable phase has a higher re-melting temperature than the phase before annealing.

Contact resistivity between both diffusion barriers and the poly-Si layer is measured using a Transfer Length Method (TLM). For this measurement, "ladder" structures were fabricated on 6"-wafers and then measured using a 4-probe measurement method. The contact resistivity of the TiW-based and Ta-based diffusion barriers is relatively stable up to 500 °C annealing allowing that both diffusion barriers could be applied for μTEGs operating at high temperatures.

Kurzfassung

In der Mikrosystemtechnologie kann ein thermoelektrischer Generator (TEG) als Mikrostrukturen (μTEG) mittels einer Silizium-Oberflächenmikromechanik von hergestellt werden. Einer Poly-SiGe-Halbleiter ist ein geeignetes thermoelektrisches Material, um die Umwandlung der Wärme bis zu 600 °C in den elektrischen Strom zu ermöglichen. Jedoch ist nach bestem Wissen und Gewissen des Autors bisher keine Entwicklung eines μTEG für diese Hochtemperaturanwendungen veröffentlicht worden, weil die Zuverlässigkeit und die Stabilität der vereinigenden Materialien, z. B. eine elektrische Verbindungsleitung zwischen Poly-SiGe-Strukturen, für solche Annwendungen herausfordernd sein kann. Diese Verbindungsleitung kann mittels eines Waferbondverfahrens gefertigt werden, wobei *p*-Poly-SiGe-Säulen auf einem Wafer mit *n*-Poly-SiGe-Säulen auf anderem Wafer gebondet werden. Diese Technik erfordert ein Bondlötmittel, dessen Komponenten auf einer Plating-Base abgeschieden sind. In Bezug auf Hochtemperaturanwendungen darf das Bondlötmittel bis zu 600 °C Wärme nicht schmelzen und muss leitfähig bleiben, und die Plating-Base muss eine hohe thermische Stabilität aufweisen, d. h. sie muss Diffusion der Materialien in die Halbleiterschicht verhindern (Diffusionsbarriere), und muss auch leitfähig bleiben.

Aus diesem Grund werden TiW- und Ta-basierte Diffusionsbarrieren, die als die Plating-Base dienen, und das Waferbonden von einer Nickel-Zinn-transienten Flüssigphase (Ni-Sn-TLP) intensiv entwickelt. Beide Diffusionsbarrieren sind in Form von gestapelten dünnen Schichten mit einer Ni-Oberschicht auf 8"-Wafern hergestellt. Materialanalytische Methoden; XRD-, TEM-, TEM-EDX-, EFTEM-, SEM-EDX-Analysen, und 4-Punkt-Schichtwiderstandsmessung, sind vor und nach einem Tempern durchgeführt, um die hohe thermische Stabilität der beiden Barrieren zu überprüfen. Das Tempern wird in einer Vakuumkammer bei angegebenen Temperaturen bis zu 600 °C für 24 h durchgeführt. Nach diesem Tempern wird keine Materialdiffusion in das Si-Substrat oder in die Poly-Si-Schicht festgestellt. Beide Barrieren weisen eine tolerierbare Zunahme des Schichtwiderstands auf.

Beim Ni-Sn-TLP-Waferbonden werden Ni- und Sn-Strukturen auf einem 6"-Waferpaar mittels einer selbstgebauten labormäßigen Galvanikanlage und eines gepulsten elektrischen Stroms galvanisiert. Dieses gepulste Galvanikverfahren kann die Dickengleichmäßigkeit der Ni-Strukturen sowie die Oberflächenrauheit der Sn-Strukturen verbessern. Für die Plating-Base werden die TiW- und Ta-basierten Diffusionsbarrieren mit der Ni-Oberschicht verwendet. Nach dem Waferbonden wird der Schertest bei einer Anzahl von ausgewählten Chips durchgeführt, um die mechanische Festigkeit des Bondlötmittels zu untersuchen, und werden Daisy-Chain-Chips elektrisch gemessen, um die elektrische Stabilität des Bondlötmittels zu untersuchen. Diese Untersuchungen werden vor und nach dem Tempern durchgeführt. Kein Umschmelzen des Bondlötmittels nach dem Tempern ist beobachtet. Das Ni-Sn-Bondlötmittel weist eine relative hohe Haftfestigkeit vor und nach dem Tempern auf und der elektrische Widerstand der Daisy-Chain-Struktur weist eine tolerierbare Zunahme nach dem Tempern auf. Die Ni-Sn-Phase des Bondlötmittels verwandelt sich in die neue stabile Phasen nach dem Tempern. Gemäß dem Ni-Sn-Phasendiagramm besitzen diese Phasen eine höhere Wiederschmelztemperatur als die Phase vor dem Tempern.

Der spezifische Kontaktwiderstand zwischen beiden Diffusionsbarrieren und der Poly-Si-Schicht ist mittels einer Transfer-Length-Methode (TLM) bestimmt. Hierzu werden die "Leiter" Strukturen auf 6"-Wafer gefertigt und mittels eines 4-Punkt-Messverfahrens gemessen. Nach dem Tempern bis zu 500 °C ist der spezifische Kontaktwiderstand der TiW- und Ta-basierten Diffusionsbarrieren relativ stabil. Dieses Ergebnis bestimmt, dass beide Barrieren für die Hoch-

temperatur-μTEGs verwendet werden können.

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List of Abbreviations

a-C	Amorphous Carbon
c-Si	Single crystalline silicon
dc	duty cycle
e.g.	*exempli gratia* : for example
i.e.	*id est* : that is
ALD	Atomic Layer Deposition
BMBF	Bundesministerium für Bildung und Forschung
CTE	Coefficient Thermal Expansion
Cu-Sn TLP	Copper-Tin Transient Liquid-Phase
CVD	Chemical Vapor Deposition
DC	Direct Current
DI water	Distilled water
EBR	Edge Bead Removal
EDX	Energy Dispersive X-ray
EEL	Electron Energy-Loss
EELS	Electron Energy-Loss Spectroscopy
EFTEM	Energy Filtered Transmission Electron Microscopy
EHT	Extra High Tension
EKC830	N-Methyl Pyrrolidinone, 2-2 Aminoethoxy Ethanol
FEG	Field Emission Gun
FhG-ISiT	Fraunhofer Institute for Silicon Technology
HAADF	High-Angle Annular Dark Field
HAc	Acetic acid
HMDS	Hexamethyldisilazane
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IGBT	Insulated-Gate Bipolar Transistor
IMC	Intermetallic Compound
JCPDS-ICDD	Joint Committee on Powder Diffraction Standards of the International Center for Diffraction Data
MEMS	Microelectromechanical System
NDL	Nernst Diffusion Layer
Ni-Sn IMC	Nickel-Tin Intermetallic Compound
PDL	Pulse Diffusion Layer
Poly-Si	Polycrystalline Silicon
Poly-SiGe	Polycrystalline Silicon Germanium
PVC	Polyvinyl chloride

PVD	Physical Vapor Deposition
RER500	Mixture of methyl-ethyl-ketone and ethyl-lactate
RF	Radio Frequency
RT	Room Temperature
SEM	Scanning Electron Microscopy
SiEGeN	Silizium basierte Hochtemperatur-Thermogeneratoren auf 8“-Wafer-Level
SSDL	Steady-State Diffusion Layer
STEM	Scanning Transmission Electron Microscopy
TE	Thermoelectric
TEG	Thermoelectric Generator
TEM	Transmission Electron Microscopy
TLM	Transfer Length Method
TLP	Transient Liquid-Phase
UV	Ultra violet
XRD	X-Ray Diffraction
µTEG	Microthermoelectric Generator

Chapter 1

Introduction

As the world population increases, energy consumption will also increase. This increase is not equivalent to an increase in energy availability. It is just a matter of time before fossil energy resources are depleted. In Germany, this situation is exacerbated by the government's policy of shutting down all nuclear power plants by 2022 [1]. The increase in energy consumption, especially of electrical power, cannot be avoided because people need energy for their daily activities. Industry, transportation, and use of household appliance are three of the most significant areas which the people's activities consume a lot of energy. In order to increase the energy availability, alternative (renewable) energy resources, *e.g.* solar energy, wind energy, geothermal, and etc. can be utilized. However, the energy production from these types of resources cannot meet the world's demand for energy because this demand is increasing at a faster pace than the increase in availability as a result of the exponential growth of the world population. Therefore, another energy resource, *i.e.*, from waste energy, needs to be found urgently to increase energy availability.

The energy produced from a waste energy resources can be generated by converting waste heat into electrical power. Waste heat can be found, for examples, in industrial pipelines for flowing hot gasses or fluids, in hot parts of a combustion engine in transportation vehicles, and in the burning gas from a kitchen stove appliance. To convert waste heat into electrical power, a technological application - a so-called thermoelectric generator (TEG) has been developed in macro and micro sizes [2]. By integrating a TEG into a device consisting of a sensor and a transmitter, the electrical power for operating the device will be provided by the TEG. If this device uses a rechargeable battery, the electrical current for recharging the battery will be supplied from the TEG, so that the device can work without maintenance, where the plant processes stop temporarily in order to recharge the battery externally or to replace with a new battery. This TEG integration is very advantageous for industries and aircraft manufacturers because it can reduce maintenance cost and the weight of the aircraft significantly [3, 4]. In the kitchen stove appliance, a TEG generates the electrical current required for a stand-alone operation.

The conversion from heat to electrical power is based on the temperature-sensing principle of a thermocouple. This principle is known as the Seebeck effect. If two thermoelectric (TE) materials with different Seebeck coefficients are joined at one end and then the joint is heated, there will be a self-generated potential difference between the two other ends. In order to increase this potential difference, a number of thermocouples can be connected into a series to form a so-called thermopile [5]. If a device or a battery is connected to the output voltage of a thermopile, then the thermopile will supply electrical power to operate the device or recharge the battery. Figure 1.1 illustrates a thermocouple and a thermopile, and their working principle.

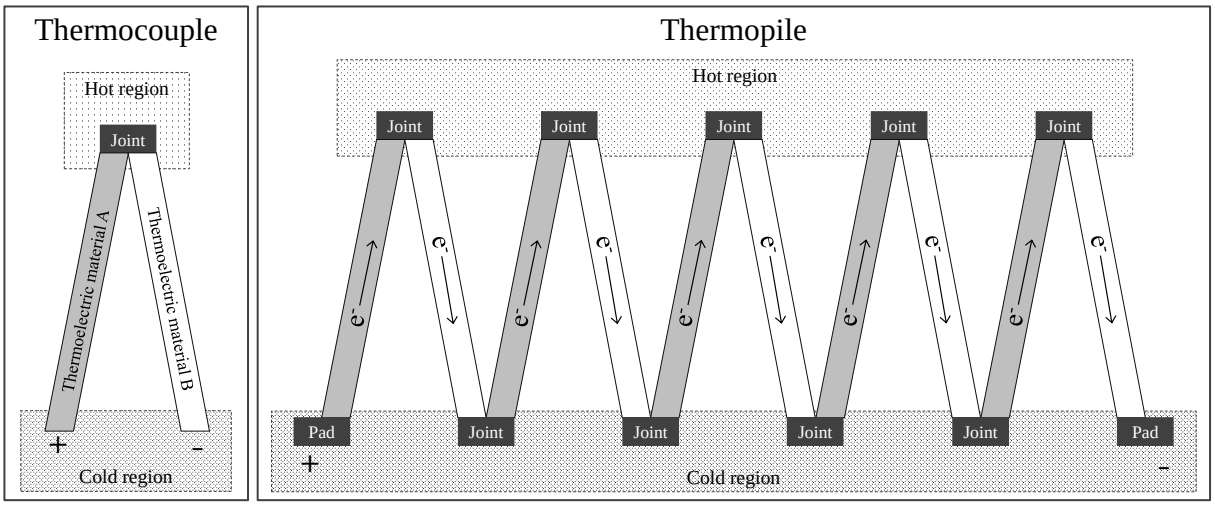

Figure 1.1: Sketches of a thermocouple and a thermopile, and their working principle.

Three properties, which determine the performance of a TE material in an application at elevated temperatures T, are Seebeck coefficient α, electrical conductivity σ, and thermal conductivity κ. Their relation is expressed as the material's figure of merit $zT = (\alpha^2 \sigma T)/\kappa$. A high zT can be met in semiconductors because they have relatively high α and low κ although their σ is lower than metals [6,7]. Figure 1.2 shows the relation of these properties that determine zT based on the material types. The applied and commercialized TE materials have $zT \approx 1$, which has been a practical upper limit [8] for over 50 years.

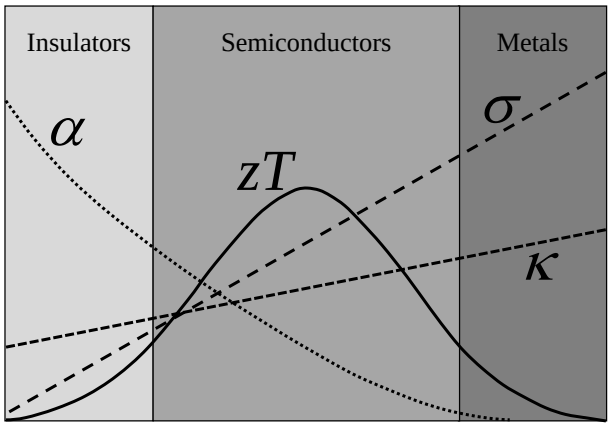

Figure 1.2: Profile of zT based on the material types, *e.g.*, from insulators having low carrier concentration to metals having high carrier concentration. The profile is adopted from [6].

1.1 Background

1.1.1 Thermoelectric generator for high temperature applications

In microsystem technology, a TEG can be fabricated in a micro-scale structure (μTEG) using a surface silicon micromachining [9–11]. A number of TE materials had been developed and their zTs were determined for TE applications. Figure 1.3 shows the zTs of several developed

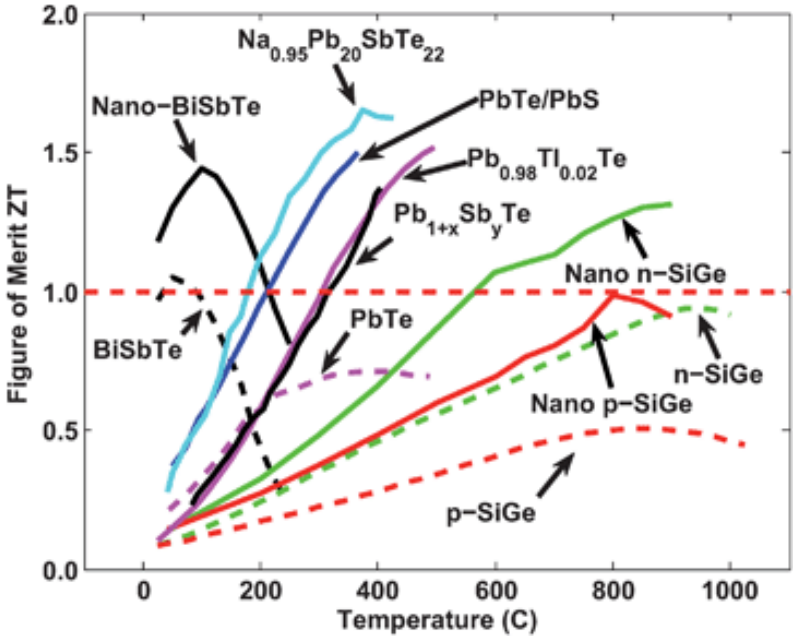

Figure 1.3: Figure of merit zT of current state-of-the-art thermoelectric materials *versus* temperature. The dashed lines show the maximum zT values for bulk state of the art materials, and the solid lines show recently reported zT values, many of which were obtained in bulk nanostructured materials. (BiSbTe, $Na_{0.95}Pb_{20}SbTe_{22}$, PbTe/PbS, $Pb_{0.98}Tl_{0.02}Te$, $Pb_{1+x}Sb_yTe$, nano *n*-SiGe, nano *p*-SiGe) [8]. The permission to reuse the figure has been granted by the Royal Society of Chemistry under a license 3697000154913.

TE materials. A well-established and commercialized μTEG is based on bismuth-telluride (BiTe) of a TE material, which operates efficiently around room temperature (27 °C), produced by Micropelt GmbH [12]. Near room temperature, both *p*- and *n*-type Bi_2Te_3 exhibit $zT \approx 0.6$ as depicted in Figure 1.3. Some developments of TE materials could have enhanced $zT > 1$ by fabricating a bulk nanostructured material. However, there are at least three challenges in developing such materials: firstly, in fabricating a material by combining the nanoparticles into a fully dense solid, secondly, in adjusting of fabrication's parameter to improve zT, and thirdly, in retaining the nanoscale structures while being used in a practical device [8]. For converting high temperature heat up to 600 °C, a semiconductor of a poly-silicon germanium (poly-SiGe) could be a suitable TE material. As shown in Figure 1.3, a TE material made from a poly-SiGe layer can have a zT, which ranges over a wide temperature from 400 °C to 1000 °C. At these elevated temperatures, the poly-SiGe TE material exhibits $zT \approx 0.6$ to 0.7 and an exceptionally high thermal stability (at ~1200 K), which leads to the usability of the poly-SiGe material in an application in deep-space probes [13]. Furthermore, the poly-SiGe material has a compatibility in the surface and bulk micromachining processes [9, 10, 14–17], that makes the poly-SiGe material an attractive thermoelectric material for a μTEG fabrication.

To the best of the author's knowledge, the applications and the developments of a μTEG for high temperature up to 600 °C have not been published or commercialized yet. A possible reason for this is that they could be limited to the incorporating or supporting materials, which are integrated in a μTEG device. Such incorporating material for the metallization of an interconnection between poly-SiGe structures can be a challenge because not all metallic materials are stable for high temperature applications. Some work has been done on developing the poly-Si or poly-SiGe materials for μTEG applications [10, 16, 17], however, it has utilized

aluminum, which is not stable against high temperature, for the interconnection. An example of a TEG module, which functions at high temperature and is available on the market, is made from an oxide for its thermoelements and is capable of converting heat up to 800 °C, however, the module's size is too large ($65 \times 65\,\mathrm{mm}^2$) [18] for the integration into microsystem technology applications.

In Germany, the development of a μTEG using the poly-SiGe material as the TE material for high temperature applications started at the beginning of 2011. The government, through *Bundes Ministerium für Bildung und Forschung* (BMBF), has established a national joint project called SiEGeN (*Silizium basierte Hochtemperatur-Thermogeneratoren auf 8"-Wafer-Level*) in order to fabricate the world's first thermoelectric generators (TEG) with a high power density up to 600 °C on a Si substrate using a developed scalable manufacturing process at a wafer-level. These TEGs have been integrated in parallel in three pilot applications in the areas of indus-

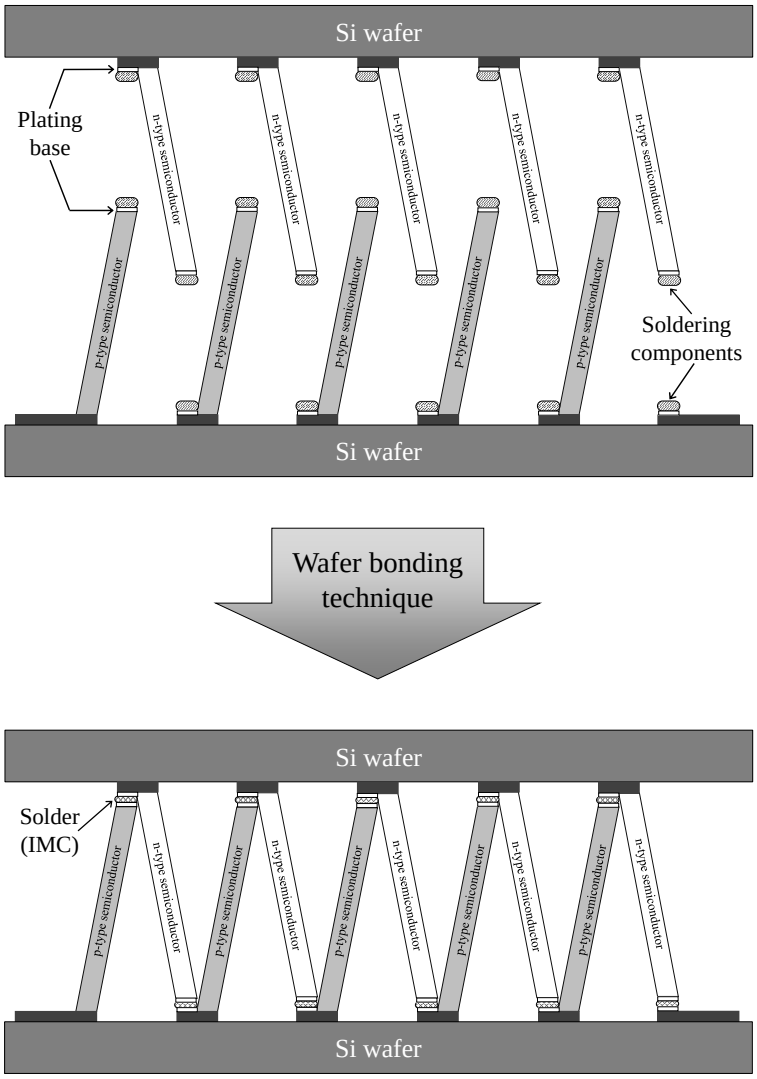

Figure 1.4: Sketch of a wafer bonding technique for creating thermopile joints. Generally, the joint is a solder made from two or more components, which are deposited on a plating base on the top of semiconductor legs on both wafers. As both wafers were bonded at a given temperature, a component of the solder was melted and mixed chemically with another layer creating a so-called intermetallic compound (IMC) layer.

trial process measurement technologies, household appliances, and aeronautics, and tested in application-specific demonstrators. The focus of this project was to develop a low-cost 8"-wafer technology platform through a combination of fundamentally-known individual processes for the high temperature material (SiGe) and to demonstrate the practical usability of the developed TEGs in the pilot applications of the above-mentioned areas. The scalable manufacturing process of a TEG fabrication was based on a wafer bonding technique, where a Si wafer containing *p*-type semiconductor legs was bonded with a Si wafer containing *n*-type semiconductor legs together as illustrated in Figure 1.4.

Nevertheless, there are a number of high temperature applications in the microsystem technology other than μTEG. Such applications can be found in space and aeronautic applications, sensors for industrial plants, etc. These applications demand a stable and reliable interconnection of an (IC) integrated circuit at high temperatures. Therefore, a new material must be developed in order to fulfill the requirement of thermally stable and reliable interconnection.

1.1.2 Scope of the investigation

It is mentioned above, the incorporating materials, *i.e.*, the interconnection between poly-SiGe structures, must be stable and withstand high temperatures. In this study, based on the fabrication method of μTEG using wafer bonding, the interconnection consists of a solder deposited on a plating base. The solder is formed during wafer bonding by mixing two or more components to create an intermetallic compound (IMC layer). The plating base is a conductive layer for depositing these components electrochemically and consists of a seed layer and an adhesion promoter. During high temperature application of at least up to 600 °C, the solder must not melt and its electrical conductivity must not decrease significantly. The plating base must maintain its electrical conductivity as well as adhesion property. Because material diffusion can easily take place at high temperature, the adhesion promoter must also prevent any diffusions into the poly-SiGe layers, so that the μTEG performance can be maintained. The presented work will focus on the high temperature reliability investigation of a barrier and a solder. The barrier will be fabricated in the form of stacked thin layers consisting of tantalum (Ta), titanium tungsten (TiW), titanium nitride (TiN), nickel (Ni). These stacked layers are deposited on a single crystalline (*c*-Si) and a polycrystalline silicon (poly-Si) substrate using two physical vapor deposition (PVD) tools, which have well-defined deposition parameters for production. The solder will be fabricated using a so-called Transient Phase Liquid (TLP) method, where a Ni layer diffuses into a melted tin (Sn) layer creating a Ni-Sn IMC solder. These Ni and Sn layers

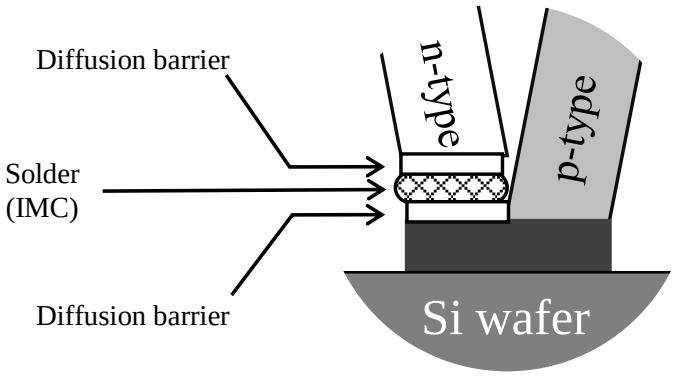

Figure 1.5: Sketch of the scope of the investigation.

are deposited using an electroplating technique which utilizes a pulsed electrical current. The fundamentals and state of the art of the barrier and the TLP-fabricated solder will be described briefly in chapter 2. The investigations were performed before and after annealing up to 650 °C. The fabrication of the barrier and the TLP-fabricated solder as well as the investigation methods will be described in detail in chapter 3. The results of the investigation will be presented in chapter 4. The discussion of the results will be presented in chapter 5. The summary and the recommendations arising from this study will be presented in chapter 6.

1.2 Objective

The aim of the study is to develop a barrier and a solder, which are reliable and applicable for high temperature application up to 600 °C.

The barrier should show a capability during high temperature annealing to prevent a material diffusion from the solder as well as from the barrier itself into the *c*-Si and poly-Si substrates. The material diffusion will be determined using X-Ray Diffraction (XRD) analysis, Transmission Electron Microscopy (TEM) analysis, and Energy Dispersive X-ray (EDX) analysis. At the same time, the barrier should maintain its electrical conductivity as well as its adhesion to the substrate against annealing. These properties will be determined using a 4-point sheet resistance measurement, an adhesive tape test, and a shear test.

The soldering components, which are the Ni and Sn layers, should be able to be deposited on Si wafers using the developed barrier as the plating base. The wafer bonding technique should be able to establish a high re-melt temperature solder. This solder should maintain its mechanical and electrical properties against annealing. These properties will be determined by performing shear tests on dies, which have a 16×16 array of $100 \times 100\,\mu m^2$ structure (mechanical characterization), and a 4-point resistance measurement on dies, which have a daisy chain structure (electrical characterization).

In respect to the TEG requirement, the impact of annealing to the contact resistivity between the barrier and the poly-Si layer should be determined using the transfer length method (TLM).

Chapter 2

Fundamentals and State of the Art

2.1 Diffusion barrier

Generally, an interconnection consists of a conductive layer and an adhesion promoter. The adhesion promoter prevents the conductive layer being delaminated from its substrate and the conductive layer serves as a path for transmitting electrical signals between micro or nano devices in ICs (integrated circuits) or in MEMS-based sensors. Figure 2.1 shows an example of an interconnection application. In an IC or a sensor fabrication, there can be a process where the conductive layer is subjected to high temperature, which could force a material to diffuse across an interface. Without a barrier layer, at high temperature the conductive layer will diffuse into the substrate and thus the interconnection will be unreliable and, in a specific case, can reduce the functionality of a substrate [19]. For this reason, an adhesion promoter must also serve as a barrier, in order to prevents a material diffusion between the conductive layer and the substrate.

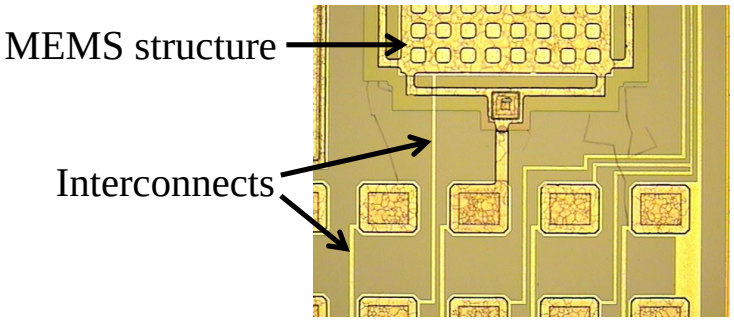

Figure 2.1: Interconnections between a MEMS structure and contact pads.

If a thin film is sandwiched between two layers, then it must fulfill some conditions in order to act as a barrier. The diffusion should not take place between both layers and the barrier. This can be determined from the diffusivity of each layer. The diffusivity of a barrier's element should be as small as possible within the sandwiching layers. At any temperatures, the barrier should not react or create a compound with the sandwiching layers. Figure 2.2 illustrates diffusion and compound formation which could possibly take place if a barrier is sandwiched between two layers. The barrier should exhibit high electrical and thermal conductivities as well as low layer stress. Contact resistance between the barrier and the sandwiching layer should be low, too [19, 20]. Nevertheless, grain boundaries or defects are always present within a thin film, thus the ideal conditions mentioned above may be compromised.

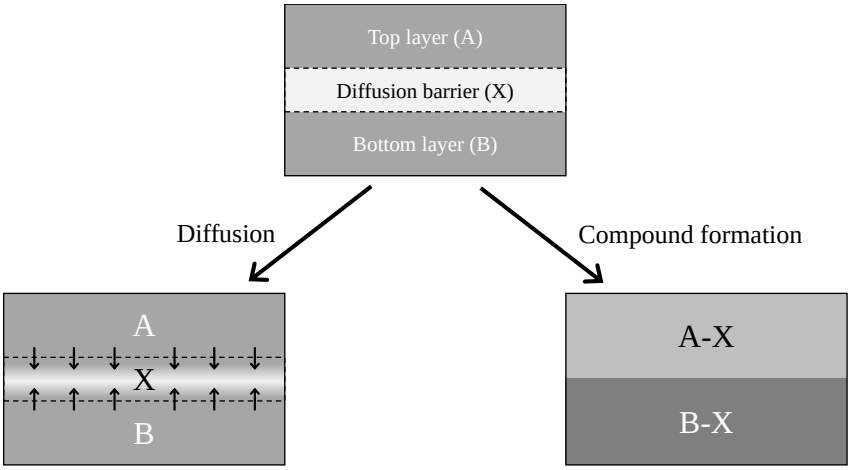

Figure 2.2: Two possible reactions if a barrier is sandwiched between two layers.

2.1.1 High temperature diffusion barriers

Each material or element has a specific diffusion coefficient, diffusivity D_0, which indicates the diffusion rate of atoms in a media, *i.e.*, in a solid, and is influenced by temperature. The temperature T [K], modifies the diffusivity exponentially D [m^2/s], which depends as well on the energy E [J/mol], required to diffuse one mole of atoms, as formulated in Equation 2.1 [21]. The gas constant R is 8.31 J/(mol K).

$$D = D_0 \exp\left(-\frac{E}{R \cdot T}\right) \tag{2.1}$$

There are numerous materials which have been investigated for barriers in the past five decades. In order to better appreciate the consequences of temperature on material diffusion, the barrier is grouped at least into five types; single element, single crystal, compound, passive compound, and "stuffed" barriers. These types are discussed in the following sections.

Single element barriers

A single metal element can be applied as a barrier because it usually exhibits a high electrical conductivity. Single element metal of Cr, Ta, W, Nb, Mo, Co, Ni, Pd, Pt, *a*-C, and Al has a temperature stability ranging from 200 to 650 °C for a barrier with Cu as a conductive layer [22]. The electrical resistivity of a Cu layer deposited on a metallic barrier has shown a stability up to 400 °C annealing for the Ti and Cr barriers, up to 500 °C annealing for the Mo and Nb barriers, and up to 600 °C annealing for the Ta and W barriers. These annealing processes were performed for 1 h [23]. A 50-nm-thick Ta barrier deposited on a Si substrate could prevent a diffusion from a Cu top layer into a Si substrate and maintain its sheet resistivity up to 630 °C annealing as it was ramped at 3 °C/min from 25 to 750 °C [24]. A 100-nm-thick Ta barrier was proposed to be deposited between a Cu top layer and an Si substrate because it could maintain the sheet resistance of the Cu top layer up to 625 °C annealing for 30 min while a 50-nm-thick and a 10-nm-thick Ta barrier could only be stable below 600 °C annealing [25]. A 30-nm-thick Ta barrier was stable up to 650 °C annealing for 35 min as it was deposited between a Cu and a SiO_2 layer. This Ta barrier was deposited using an ionized metal plasma sputter deposition in order to improve the step coverage without reducing the diffusion barrier property and to deposit a dense Ta layer microstructure, particularly at grain boundaries [26].

Single crystal barriers

In polycrystalline thin films, grain boundaries and dislocations are the paths where diffusing atoms may favorably diffuse within a thin film because in these diffusion paths, the energy for activating a diffusion mechanism is lower than in crystal lattice. Therefore, a single crystal thin film can be beneficial as a barrier because such film exhibits no grain boundaries and dislocations. However, this is not a practical solution for any application because a pure single crystal thin film can exhibit a high internal stress in maintaining its crystallinity that could lead to a poor adhesion to a substrate [20, 27, 28]. An example of a single crystal barrier is a TaN thin film deposited using a pulsed-laser deposition with a Cu top layer. This single crystal TaN barrier can prevent a Cu diffusion up to 650 °C annealing for 30 min [29] whereas a polycrystalline TaN barrier can only remain stable up to 500 °C annealing 35 min [30]. On the other hand, an amorphous thin film can also be an effective barrier, which was shown by two amorphous Ta barriers deposited using a PVD and an ALD method, for being stable up to 700 °C and 750 °C annealing, respectively, as they were ramped at 3 °C/s from 100 to 1000 °C [31].

Compound barriers

A compound or an alloy can also be a barrier due to its free energy of a compound formation. This energy must be lower than the free energy for forming a compound between the single element of the barrier and the element of adjoining layers. This relation will ensure that the barrier will be thermodynamically stable, although material diffusion from the adjoining layers into the barrier can possibly take place [20]. A 100-nm-thick TiW alloy with 19–26 at.% of Ti can prevent a diffusion from a Cu top layer into a Si substrate below 600 °C annealing for 30 s in a rapid thermal annealer [32]. A 120-nm-thick TiW alloy with 30 at.% of Ti has shown no interdiffusion with an Al top layer and exhibited a stable contact resistivity up to 500 °C annealing for 30 min [33]. A 110-nm-thick TiW alloy with 30 at.% of Ti has shown chemical stability in preventing a diffusion from a Ag top layer into a Si substrate and exhibited a stable sheet resistivity up to 600 °C annealing 1 h [34]. Another alloy, which has been investigated as a barrier, is Ta-Si alloy. A 10-nm-thick amorphous $Ta_{73}Si_{27}$ barrier can be thermally stable in preventing a diffusion from a Cu top layer into an Si substrate up to 575 °C annealing 1 h [35]. An investigation of a 10-nm-thick Ta-Si alloy with 75 at.% of Si for a metallic contact on a gate dielectric has shown a thermal stability by exhibiting a stable work function up to 1000 °C annealing for 5 s [36]. The nitride of a Ta-Si alloy was also investigated in order to prevent interaction between a conductive top layer and a GaAs substrate. It was reported that a 100-nm-thick amorphous $Ta_{34}Si_{25}N_{41}$ alloy can prevent a diffusion from a Ag and a Au top layer into an Si substrate up to 750 °C and 800 °C annealing for 5 min, respectively [37].

Passive compound barriers

Another type of barrier is a passive compound barrier, which exhibits a chemical stability and a negligible mutual solubility and diffusivity. This type of a barrier can be found among the carbides, nitrides, borides, and conductive oxides due to their large negative energy of formation. So far, the transition-metal nitrides, such as TiN, and TaN, are the most common passive barriers, which can be found in device applications [19, 20]. It was reported that a 50-nm-thick TiN barrier has effectively prevented an eutectic reaction between an Au top layer and an Si substrate at 800 °C annealing for 30 min. A sputter deposition with a deposition rate of 15 nm/min

and a substrate bias of −50 VDC was used to deposit the TiN barrier. The failure of this barrier was related to compressive stresses induced during annealing [38]. A 50-nm-TiN barrier could prevent a diffusion from a Cu top layer into a GaAs substrate and maintain its contact resistivity up to 450 °C annealing for 30 min [39]. By fabricating nearly stoichiometric composition nitride barriers, the sheet resistance of a Cu top layer can be maintained up to 600 °C and 700 °C annealing for 60 min as it was deposited on the 25-nm-thick TiN and TaN barriers, respectively [40]. A 50-nm-thick TaN barrier could show a stability up to 700 °C annealing for 1 h as it was deposited as an *fcc* crystalline phase between a Cu top layer and an Si substrate [41]. A 150-nm-thick Mo-nitride-based barrier was deposited using N_2:Ar (1:4) gas and could prevent a diffusion from an Au top layer into an Si substrate up to 450 °C annealing for 30 min. A visible Au discoloration was no longer visible after annealing at 450 °C for 30 h [42]. However, a contact resistivity of a 200-nm-thick Mo-nitride-based layer deposited using N_2:Ar (∼ 1:8) gas with an Al top layer was stable up to 402 °C annealing for 30 min [43]. A W-nitride-based barrier with a thickness ranging from 1.5 to 100 nm was deposited using an ALD technique and could prevent a diffusion from a Cu top layer into an Si substrate up to 600 °C annealing for 30 min [44]. Table 2.1 summarizes all the barriers which are mentioned above.

"Stuffed" barriers

An interesting solution is to decorate grain boundaries by introducing a suitable impurity with small concentration from $\sim 10^{-1}$ to 10^{-3} at.% during deposition of a thin film. The impurity, such as oxygen or nitrogen, could be distributed along grain boundaries so that it creates a "stuffed" barrier, which can withstand the heat treatment [19, 20]. The "stuffed" barrier was shown in a Cr barrier for preventing Au diffusion. During Au deposition, the deposition chamber was backfilled with oxygen gas for 10–18 min in order to let Cr atoms diffuse through Au grain boundaries and form Cr_2O_3 over the grain boundary surfaces. At this stage, the Au layer was stuffed with Cr_2O_3, thus its conductivity was reduced significantly. Therefore, another Au layer was deposited on this "stuffed" Au layer for the conductive layer. This additional Au layer exhibited almost no increase in resistivity at 300 °C annealing for 2 h in air [45]. Figure 2.3 illustrates the fabrication of a "stuffed" Au layer using the Cr barrier. Another example of "stuffed" barriers was shown in a 100-nm-thick W-boride-nitride thin film stuffed with a nitrogen gas. Chemical and sheet resistance stabilities can be enhanced up to 1000 °C annealing for 30 min [46]. However, the "stuffed" barriers could not be applied for a semiconductor contact because the contact resistivity between the barrier and semiconductor may be significantly high due to a high concentration of the impurities at the grain boundaries of the barriers.

There were also some investigations, which combine a pure metal thin films with a metal-nitride based barrier. This combination aimed to provide a better adhesion of a barrier on a sub-

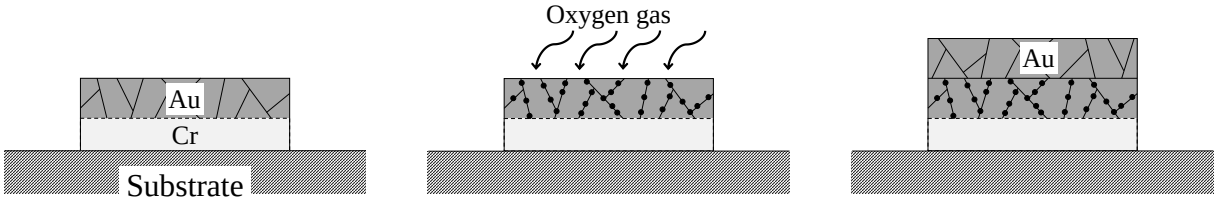

Figure 2.3: "Stuffed" barrier. After the deposition of Cr and Au layers, oxygen gas is introduced into the chamber. Through grain boundaries of Au, Cr diffuses and forms Cr_2O_3 with oxygen. Another Au layer is deposited on the top as a conductive layer.

Table 2.1: Summary of the reviewed high temperature barriers.

Barrier	Thickness [nm]	Stable Temp. [°C]	Time [min]	Top layer	Remarks
Ti	60	400	60	Cu	-
Cr	60	400	60	Cu	-
Mo	60	500	60	Cu	-
Nb	60	500	60	Cu	-
W	60	600	60	Cu	-
Ta	60	600	60	Cu	-
Ta	50	630	ramp.	Cu	-
Ta	100	625	30	Cu	-
Ta	50 & 10	<600	30	Cu	-
Ta	30	650	35	Cu	IMP deposition
Ta	14	750	ramp.	Cu	amorphous
Ta	22	700	ramp.	Cu	amorphous
TiW	100	<600	0.5	Cu	19-26 at.% of Ti
TiW	120	500	30	Al	30 at.% of Ti, contact resistivity
TiW	110	600	60	Ag	30 at.% of Ti
TiN	50	800	30	Au	-
TiN	50	450	30	Cu	GaAs substrate
TiN	25	600	60	Cu	-
TaN	-	650	30	Cu	single crystal
TaN	-	500	35	Cu	poly crystal
TaN	25	700	60	Cu	
TaN	50	700	60	Cu	*fcc* phase
Mo-N	150	450	1800	Au	-
Mo-N	200	402	30	Al	contact resistivity
W-N	1.5 - 100	600	30	Cu	using ALD
$Ta_{73}Si_{27}$	10	575	60	Cu	amorphous
Ta-Si	10	1000	5 sec.	-	75 at.% of Si, gate dielectric
$Ta_{35}Si_{24}Ni_{21}$	100	750	5	Ag	amorphous, GaAs substrate
$Ta_{35}Si_{24}Ni_{21}$	100	800	5	Au	amorphous, GaAs substrate

strate and to minimize barrier internal stresses. A Ti thin film was overlaid with a TiN thin film (Ti/TiN) and its requirement for the barrier was investigated for a Cu conductive layer [47, 48] as well as for an Al conductive layer [49]. Stacked layers of Ta/TaN as well as Ta/TaN/Ta for a barrier were investigated showing nitrogen diffusion into adjoining Ta layers at 300 °C annealing for 1 h [50]. The stacked layer of Ta/TaN was studied as well for the barrier between a Cu layer and diodes in order to improve the integrity of Cu/TaN_x/Ta/n^+-p junction diodes up to 650 °C annealing for 1 h [51].

2.1.2 Stresses in diffusion barriers

Stress classification

Thin film stresses are always present within barriers and can originate primarily from intrinsic, thermal, and mechanical stresses [52]. Intrinsic stress exists virtually although barriers are

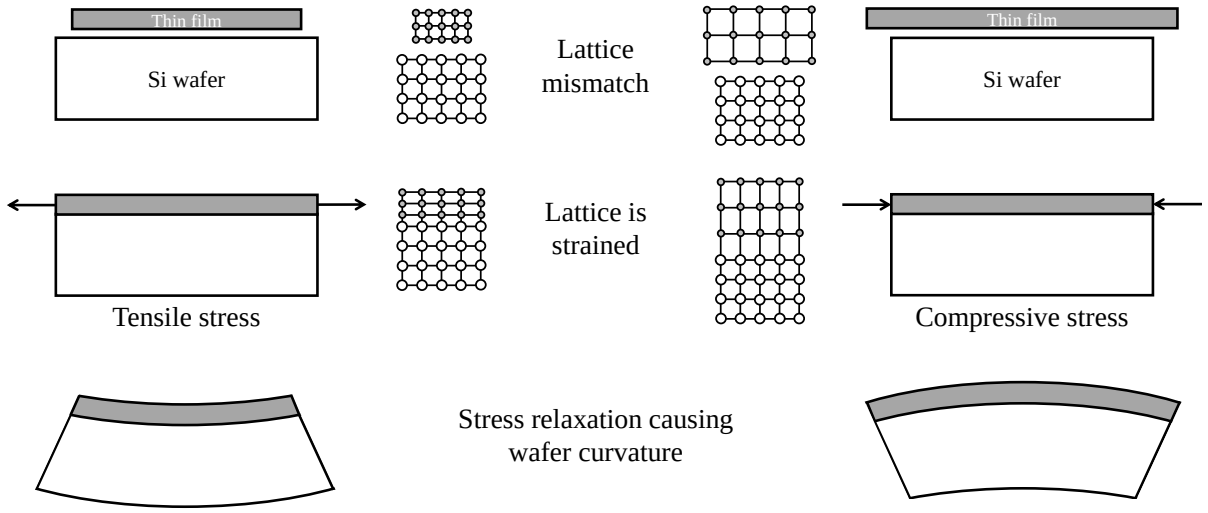

Figure 2.4: Barriers under the tensile and compressive stresses due to a lattice strain causing a wafer curvature.

not under external forces because such stresses originate from assimilated residual gas atoms during a barrier deposition, variations in the interatomic distance within a crystal size, recrystallizations, voids and dislocations, and phase transformations. These causes can be tailored by adjusting parameters of a barrier deposition technique, so that a barrier with low intrinsic stresses can be fabricated. A high intrinsic stress can affect the electrical conductivity, the diffusivity of foreign atoms, crystalline defects, and the adhesion property of a barrier. Because the intrinsic stress tends to increase as the barrier thickness increases, it is favorable to deposit a thin barrier with a defined thickness [19].

Intrinsic stress can also originate from the crystal structure difference between the barrier and its substrate (generally a single crystal Si wafer). Due to this difference, there will be a lattice mismatch between the barrier and its wafer as depicted in Figure 2.4. When a barrier is deposited on a wafer, its crystal lattice will be strained in order to let all atoms on the barrier's surface bond with Si atoms on the wafer's surface. In this situation, the barrier is under a tensile or a compressive stress, which leads to a wafer curvature at the equilibrium state, as illustrated in Figure 2.4. The tensile-stressed and compressive-stressed barriers will bend the wafer concavely upward and convexly outward, respectively. This bending of the wafer could be a problem, *e.g.*, in maintaining an accuracy tolerance for a lithographic definition of device features. Dislocations occur at an interface where atoms from the barrier do not bond with the

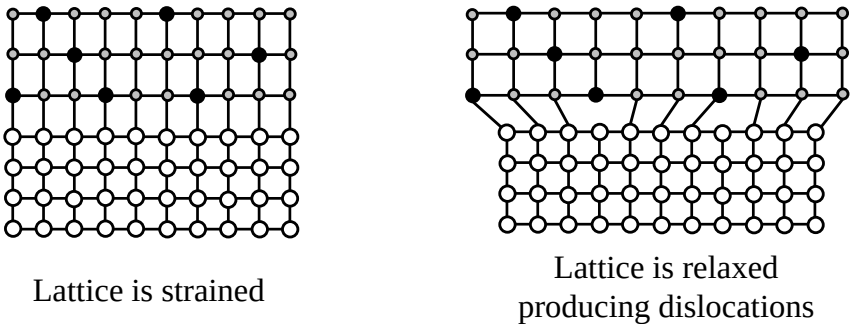

Figure 2.5: Dislocations at the interface due to relaxation of a strained barrier deposited on a substrate.

Si atoms, as illustrated in Figure 2.5, due to the lattice mismatches, also after the barrier stresses are relaxed.

Materials or barriers exhibit a thermal stress that causes a change in the barrier's dimension as they are exposed to an ambient having a temperature higher or lower than the room temperature. The significance of the dimension change is different between barriers, and depends on their thermal property, namely the thermal expansion coefficient (CTE). During wafer processing, a wafer is usually exposed to a non-uniform heating or cooling in several processing steps. A process failure will arise due to an expansion or a shrinkage of the barrier that leads to a delamination of a barrier from its substrate. Therefore, it is important to select a barrier having a CTE, which is close to the CTEs of the adjoining or incorporated layers. Table 2.2 lists CTEs of given thin films at room temperature.

Mechanical stress is a result when a barrier is under mechanical (as opposed to thermal) loads: compression or expansion [52].

Table 2.2: List of CTEs of given thin films at room temperature [53].

Material	CTE [ppm/K]	Material	CTE [ppm/K]
Si	2.6 - 3.3	Au	14.0
W	4.5 - 4.6	Ag	19.0
Mo	4.8 - 5.1	In	20 - 33
Ge	6.0	Cu	16.5 [54]
Ta	6.5	Al	23.6 [54]
Cr	4.9 - 8.2	TiN	8.5 [55]
Ti	8.4 - 8.6	TiW	4.5 - 8.6 [56]
Pt	8.8 - 9.1	TaN	24.5 [57]
Ni	13.0		

Stress adjustment

Since the late nineties, Ta, TiN, TaN, and TiW thin films have become of great interest for barrier investigations due to their low solubility with a Cu conductive layer and high chemical stability with dielectric layers or Si substrates at high temperature. The effects of heat treatment in regard to the internal stresses of barriers have also been thoroughly investigated. A barrier stress can be suppressed low by modifying the deposition parameter of a barrier so that diffusing atoms within a barrier can exhibit a low diffusivity, for an example the low diffusivity of indium atoms through a 100-nm-thick TiW barrier [58]. Intentionally, a thick barrier could be deposited in order to block the diffusing atoms from a top layer in reaching the substrate. For example, a 100-nm-thick Ta barrier could be deposited in order to form a Ta silicide at Ta/Si interface during 650 °C annealing. The Ta silicide layer may block and prevent a diffusion from a Cu top layer into the substrate [59]. However, a thick barrier could exhibit a high tensile stress and could be problematic due to a high induced thermal stress upon high temperature applications. The barrier stress can be managed by selecting an appropriate barrier to be deposited. A 30-nm-thick barrier with a 10-nm-thick Cu top layer could exhibit low stress if a Ta or a *c*-TaN barrier was used whereas an amorphous TaN or a CVD TiN barrier could lead to high stress [60]. Stacking thin films could also be fabricated in order to improve a barrier's adhesion to a substrate, for example a TaN barrier was deposited on a Ta barrier. However, this stacking TaN/Ta barrier could exhibit a high sheet resistance due to the high resistivity of the TaN layer.

Interestingly, a barrier can be sandwiched with another two barriers, so that the sheet resistance of the barrier can be maintained low. For example, a TaN barrier was sandwiched with two Ta barriers for improving the thermal stability of a barrier [50].

Another possible way to fabricate a thick barrier with a conductive top layer having low stress, is to co-deposit a tensile-stressed thin film with a compressive-stressed thin film. A TiN barrier can be applied for the compressive-stressed thin film and this stress was irreversibly decreased up to 800 °C annealing [55]. With these stacking tensile-compressive-stressed thin films, the barrier stress can be optimized in order to minimize the wafer curvature. This barrier type can be fabricated by sandwiching a 100-nm-thick TiN barrier with a TiW or a Ta barrier, which exhibits a tensile stress. It has shown that these two barrier types could prevent a diffusion from an Ni top layer into an Si substrate and maintain their sheet resistance up to 600 °C annealing [61].

Stress influencing barrier's electrical resistivity

Electrical resistivity is determined by the scattering of electrons due to the presence of defects within a thin film such as impurities, dislocations, and grain boundaries. The annihilation of these defects reduces the barrier's resistivity. Upon annealing, the impurities segregate via grain boundaries to the barrier surface and/or to the barrier-substrate interface. This segregation unpins the grain boundaries, leading to a grain growth of the barrier's grains. Dislocation glides are activated as well so that a barrier stress is relaxed. During grain growth, coarsening of the barrier's grains starts with the growth of a few grains, which consume the surrounding fine-grained matrix until the large grains meet and the fine-grained matrix is completely consumed. The resistivity is decreased during grain growth because the scattered electrons are reduced by the diffusion and coalescence of impurities at the grain boundaries, by the decrease of dislocation concentration, and by the reduction of the grain boundaries. However, the grain growth leads to the annihilation of excess volume by reducing the amount of the grain boundaries which induces a shrinkage of the barrier. This gives rise to tensile stress if the barrier remains bonded to the substrate [62]. In a tensile-stressed barrier, crystal lattices undergo plastic deformation, which introduces new dislocations within the lattices, therefore electrons are again scattered and thus, increase the resistivity [63].

2.2 Transient-liquid phase wafer bonding

Wafer bonding is a part of the microsystem technology which is aimed commonly to encapsulate semiconductor and MEMS devices. These devices are usually very sensitive to an environment, therefore a hermetic encapsulation is required for proper operation. Such an inertial sensor, fabricated using a Si micromachining, works under a defined surrounding ambient pressure in order to provide a near-critical damping. Here, the role of the wafer bonding is to enclose the inertial sensor inside a cavity with a defined cavity's ambient pressure [64–66]. Wafer bonding technology is classified based on the types of the bond material as shown in Figure 2.6 [65].

In respect to the focus of the study, the wafer bonding with metallic intermediate layers (metal-metal bonding) is suitable for the reliability investigation for high temperature applications. Furthermore, a TLP wafer bonding provides a better solution because it can be established at low temperatures, typically below 300 °C (see Table 2.3 below), in creating a bond solder having a high melting temperature. The TLP wafer bonding becomes more attractive because it can

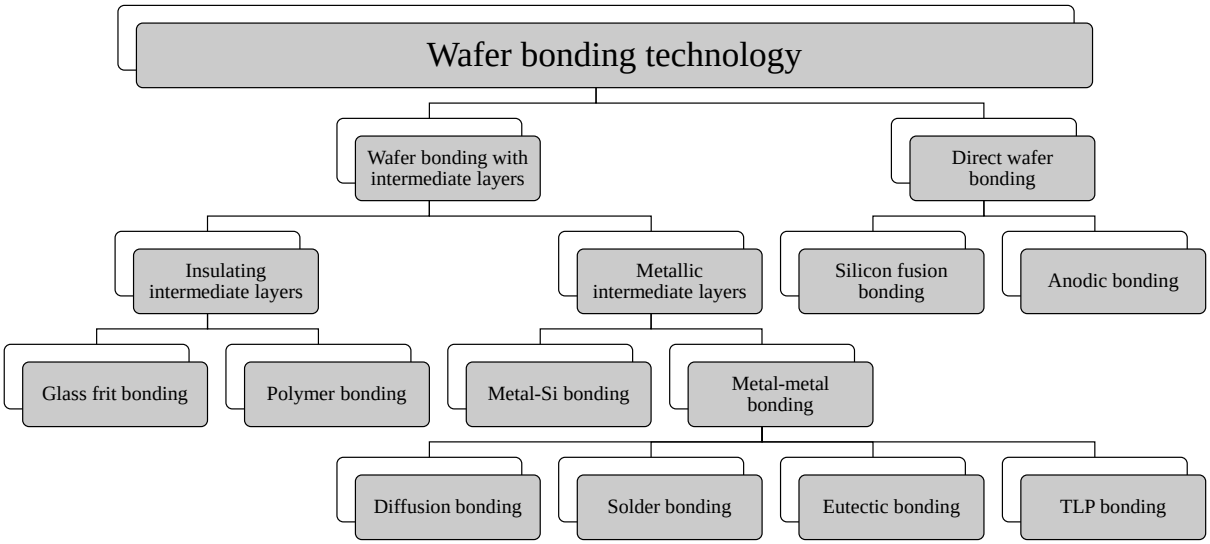

Figure 2.6: Classification of the wafer bonding technology.

utilize a low cost technique to deposit TLP bond solder components, *e.g.*, using electroplating method, and the TLP bond solder can be flowing over non-planar surfaces, *e.g.*, due to electrical feedthroughs, during wafer bonding [67].

A bond solder component material which has a low melting temperature (interlayer), *e.g.*, Sn or In, melts and then interdiffuses with the other component (parent metal), *e.g.*, Cu, Ag, Au, or Ni until an IMC or a TLP bond solder with high melting temperature grows. Before wafer bonding, the parent metal is deposited on the top and the bottom wafers followed with the interlayer deposition. In order to describe the TLP bond solder formation briefly during wafer bonding, a model of solder component interactions was proposed [75, 76]. The model divides the interactions into four stages, which is illustrated in Figure 2.7 for the Ni-Sn TLP bond solder. At stage 1, bond structures from each wafer are in contact followed by heating up the system beyond the melting temperature of the interlayer (Sn layers). During heating up, the interdiffusion is already taking place between the parent metal (Ni layers) and the Sn layers. Therefore, it is important to have a high heating rate in order to reach a high diffusivity of Sn atoms into the Ni layers. Otherwise, the interdiffusion is stopped due to an early Ni-Sn IMC formation that inhibits further interdiffusion. At stage 2, the Sn layers melt, filling the voids or pores on the Ni layer's surface and covering up the non-planarities of wafer topographies. It

Table 2.3: Formation and remelting temperatures of several TLP bond solder components. Question mark means no investigation has been performed using wafer bonding technology.

Metal-metal for TLP wafer bonding	Bond temp. [°C]	Remelt Temp. [°C]	Voids free and hermetic sealing	High bond strength
Cu – In	180	> 307	?	?
Cu – Sn	280	> 415	?	Yes [68]
Ag – Sn	250	> 600	Yes [69]	?
Ag – In	175	> 880	Yes [70]	?
Au – Sn	260	> 278	Yes [68]	Yes [68]
Au – In	200	> 495	Yes [67, 71]	Yes [72, 73]
Ni – Sn	300	> 400	Yes [74]	Yes [73]

is important to deposit sufficient Sn layers in order to keep the molten Sn layers available for growing the Ni-Sn IMC further, so that both wafers can still be moved to one another during wafer bonding, thus, the non-planarities of wafer topographies are sealed completely. At stage 3, the Ni-Sn IMC grows and all molten Sn layers with a sufficient thickness are consumed. The melting temperature of the Ni-Sn IMC has now changed from the melting temperature of the Sn layers to the lowest melting temperature of all available IMC phases grown within the bond solder. At stage 4, the Ni-Sn TLP bond solder (Ni-Sn IMC and unconsumed Ni layers) is heated at a temperature higher than the melting temperature of the Sn layers, but not higher than the remelting temperature of the grown Ni-Sn IMC. With this heating, all the unconsumed Ni layers will be converted to the Ni-Sn IMC layer, so that the Ni-Sn TLP bond solder has a homogeneous Ni-Sn IMC phase, which increases the mechanical strength of the bond solder [77].

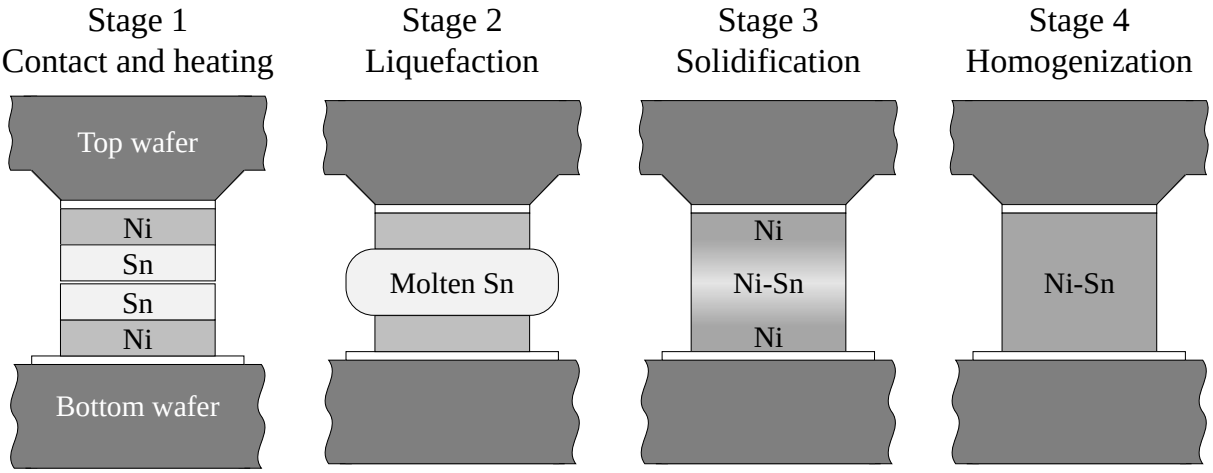

Figure 2.7: Interaction between interlayer (Sn layers) and parent metal (Ni layers) during the Ni-Sn TLP wafer bonding.

2.2.1 TLP bond solder for high temperature applications

The investigations of metal-metal intermediate layers shown in Table 2.3 above were performed especially for TLP wafer bonding. In these investigations, whether the TLP bond solders has a higher melting temperature than the fabrication/bond temperature wes not reported. Except for the Au-In intermediate layer, the TLP bond solder was annealed at 400 °C for 1 h to check whether the solder had melted [73]. The melting temperature of a TLP bond solder consisting of a compound of those intermediate layers may simply be estimated by studying the corresponding the compound phase diagrams. Table 2.4 summarizes the stable phases which have the highest and the lowest melting temperatures, that can possibly be grown within a TLP bond solder from the given intermediate layers.

Heat treatment at 600 °C will cause re-melting of the TLP bond solder due to the presence of a stable phase which has a lower melting temperature than 600 °C. Table 2.4 shows the compounds of the TLP bond solder, which has a stable phase that already melts at 600 °C annealing, except, the phases of the Ni-Sn compound. To avoid melting of the TLP bond solder, the thickness of the parent metal and the interlayer can be estimated using a proposed Equation 2.2 [73].

$$\frac{h_{\mathrm{PM}}}{h_{\mathrm{IL}}} = \frac{\rho_{\mathrm{IL}}}{\rho_{\mathrm{PM}}}\left(\frac{1}{\mathrm{wt.\%}} - 1\right) \tag{2.2}$$

Table 2.4: Stable phases having highest and lowest melting temperatures based on the corresponding phase diagrams [78].

Compound of TLP bond solder	Stable phases	Melting temperature [°C]	Concentration of interlayer [wt.%]	h_{PM}/h_{IL}
Cu – In	β	710	28.5 – 37	2.05 – 1.39
	$Cu_{11}In_9$	310	~59	
Cu – Sn	β	798	22 – 27	2.91 – 2.22
	η	415	59 – 60.9	
Ag – Sn	ζ	724	12.8 – 24.6	4.78 – 2.15
	ε	480	25.5 – 27	
Ag – In	β	695	26.2 – 31.3	1.96 – 1.53
	$AgIn_2$	166	68	
Au – Sn	$Au_{10}Sn$	532	5.7	6.31
	$AuSn_4$	217	71	
Au – In	α_1	650	7.4 – 8.9	4.74 – 3.88
	β_1	275	13.9 – 14.5	
Ni – Sn	Ni_3Sn_2	1160	54.8 – 57.9	0.68 – 0.66
	Ni_3Sn_4	794.5	71.6 – 73	

where h_{PM} and h_{IL} are parent metal and interlayer thicknesses, ρ_{PM} and ρ_{IL} are parent metal and interlayer densities, and wt.% is the mass concentration of the interlayer in the TLP bond solder after wafer bonding. In Table 2.4, h_{PM}/h_{IL} are calculated using wt.% of stable phases having the highest melting temperature. The required parent metal thickness can be determined, for example for the Cu–Sn TLP bond solder, if the Sn layer is deposited with a thickness of 1 µm, then the Cu layer must be deposited with a thickness of ~2.5 µm in order to grow a β-phase having a melting temperature of 798 °C. This thickness determination assumes that after wafer bonding the parent metal and the interlayer are completely mixed creating a compound with a homogeneous phase, which is distributed homogeneously within the TLP bond solder. A compound having a homogeneously distributed phase can only be fabricated if the mixing materials are in a powder form. However, in wafer bonding technology, both parent metal and interlayer are usually deposited in a form of layers, *e.g.*, using the electroplating method to deposit the parent metal on the substrate and then deposit the interlayer on the parent metal. In such a deposition, foreign atoms or contaminations could be incorporated within the layer of base materials, so that a compound, *i.e.*, TLP bond solder, having a homogeneously distributed phase can never be achieved.

According to the Ni-Sn phase diagram in Figure 2.8, there are three compound phases, *i.e.*, Ni_3Sn, Ni_3Sn_2, and Ni_3Sn_4, which are stable after intermixing of Ni and Sn atoms. Consequently, the Ni-Sn TLP bond solder would always contain these phases although the thickness of the Ni and Sn layers is higher than the required thickness determined by Equation 2.2. This hypothesis is also supported by the investigation of a Ni-Sn layer electroplated directly using an Ni-Sn electrolyte. The TEM-EDX and XRD analyses determined that the electroplated Ni-Sn layer consisted of Ni_3Sn_2 and Ni_3Sn_4 phases even though the Sn composition inside the electrolyte was varied in each electroplating [79]. The phase diagram indicates also that the three Ni-Sn phases could have a melting temperature above 600 °C, *i.e.*, 920.5 °C, 1160 °C, and 794.5 °C, respectively. Therefore, the application of the Ni-Sn intermediate layers will ensure

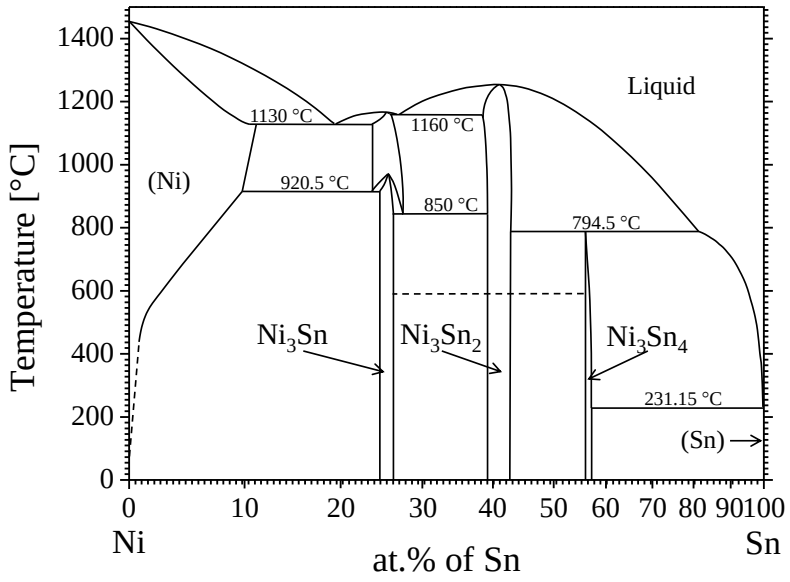

Figure 2.8: Phase diagram of the Ni-Sn compound showing three stable phases [78].

that re-melting of a fabricated Ni-Sn TLP bond solder will not occur up to 600 °C annealing. A thermal stability of a Ni-Sn TLP bond solder was shown as the Ni-Sn TLP wafer bonding was demonstrated to bond silicon IGBTs on a conventional substrate. Through this development, the Ni-Sn TLP bond solder was reliable against thermal cycling (1000 cycles; a cycle consisted of −4 °C and 200 °C for 30 min each) for high temperature power electronics in electrified vehicles [80]. The Ni-Sn TLP wafer bonding was applied to encapsulate a Pirani vacuum sensors with a titanium getter. After half a month of getter activation, the cavity pressure remained the same as the initial pressure and this pressure remained stable for several weeks [74].

The formation of a Ni-Sn compound has been studied. The compound formation was observed whether due to a dissolution of a solid Ni in a molten Sn or due to a solid-state diffusion when a Sn layer was coupled with a Ni layer. The dissolution of Ni in the molten Sn was not interfered with the growth of the Ni-Sn compound at the solid/liquid interface [81, 82]. The stable Ni_3Sn_4 phase was grown both as a layer at the solid/liquid interface and as platelets in a Sn melt. The dissolution of Ni in the molten Sn affected the growth kinetics of this phase [83]. The effect of the solid Ni dissolution in the molten Sn on the growth rate of the Ni_3Sn_4 phase was evaluated mathematically because the solid dissolution in the melt and the phase formation took place simultaneously [84]. Below melting temperature of Sn, solid-state diffusions at the joint between the Ni and Sn layers had already taken place, where Ni atoms diffused into the Sn layer growing a metastable plate-like $NiSn_3$ phase. This metastable phase was grown fast and could deteriorate the solderability of the Sn layer [85, 86]. The stable phase of the Ni_3Sn_4 compound grown at 160–200 °C was determined due to a grain boundary diffusion, which contributed to the rate-controlling process of the reactive diffusion, and due to the grain growth, which occurred at certain rates [87, 88]. The growth rate of the Ni_3Sn_4 phase at 180–220 °C increased when the Ni layer contained phosphorus or boron atoms with given concentrations [89, 90]. The hardness and the elasticity modulus of the Ni_3Sn_4 compound were 7 GPa and 134 GPa, respectively, and changed due to a residual stress development within the compound layer after 150 °C and 200 °C annealing for 24 h. The layer density was increased after 100 °C, 150 °C and 200 °C annealing for 24 h causing a significant increase in the fracture toughness of the Ni_3Sn_4 compound [91].

2.2.2 Electroplating of Ni and Sn layers using pulsed electric current

Basics

If an electroplating employs an insoluble anode, *e.g.*, platinized titanium anode, then the deposited metal atoms come from the bulk electrolyte, where the metal salts dissociate to form electrically charged anions and cations. These ions can be metal cations, positively charged complex ions or hydrogen ions, ionized acid species, negatively charged complexes or hydroxyl anions. During electroplating, *e.g.*, applying an electrical current from an external source between two electrodes, the anions are attracted to the positively charged electrode (anode) and accumulated at the insoluble anode, so that their concentration remains the same for the duration of electroplating. For the metal cations, they are attracted to the negatively charged electrode (cathode) and, close to the cathode's surface, removed by their reaction so that the concentration of metal ions is lower on the surface than in the bulk electrolyte. This concentration gradient drives the diffusion process of metal ions and the distance or the thickness of the "diffuse layer", also known as Nernst Diffusion Layer (NDL), would be approx. 0.2 mm and μm without and with forced convection, respectively.

The reaction on the cathode's surface, where the metal ions are removed, can be understood as follows. At the cathode's surface, an adsorbed layer of oriented water dipoles is formed spontaneously before metal ions reach the surface. The partially positive ends of water dipoles are attracted to the cathode's surface. Hydrated organic molecules or surface-active anions are mostly present within the electrolyte. Due to their greater ionic radius, they are easily dehydrated. Consequently, they may also be attracted to the partially negative ends of water dipoles, which are already bonded electrostatically with the electrons on the surface, and displace the adsorbed water layer and they thus are adsorbed on the surface. These anions are strongly adsorbed at the cathode so that they approach the surface more closely than the hydrated metal ions, whose hydration sheaths prevent a closer approach. While retaining their hydration sheaths, the metal ions are adsorbed at the cathode's surface by coulombic forces. This concept is known as the Stern-Graham model of the electrolyte double-layer, which is illustrated in Figure 2.9-*top*. The magnitude of the coulombic forces depends on the electrical current applied to the electrochemical cell. If the current is sufficient to attract the metal ions closely, then the hydration sheath surrounding the metal ions will be deformed or may split sufficiently wide open. Therefore, the metal ion can travel through the rigid Helmholtz layer and come close enough to the cathode's surface for the charge transfer to take place. The charge transfer takes place by tunneling the electrons from the cathode side through the Helmholtz layer and triggering the discharge process. After the charge transfer is established, the metal ions are deposited and then recrystallized for layer growth on the cathode's surface and becomes negatively charged and thus the metal ions in the bulk electrolyte are continuously attracted to the cathode.

In electroplating, the electrochemical reaction is governed by Faraday's law expressed as

$$Q = I\,t = \frac{n\,F\,W}{M} \tag{2.3}$$

The reaction at an electrode is proportional to the electric charge Q [C] generated through an electrochemical cell. This charge is equal to the electric current I [A], which passes through the cell for a given time t [s]. It defines that the weight W [g] of deposit at the cathode is proportional to the product of I and t and depends on the number n of electrons involved in the reaction and on the atomic weight M [g/mol] of deposited material as the Faraday constant

F (96.485 C/mol) applies. The actual weight W_a of deposit is always less than the calculated weight W_T, because the applied current is not only used for depositing a metal at the cathode

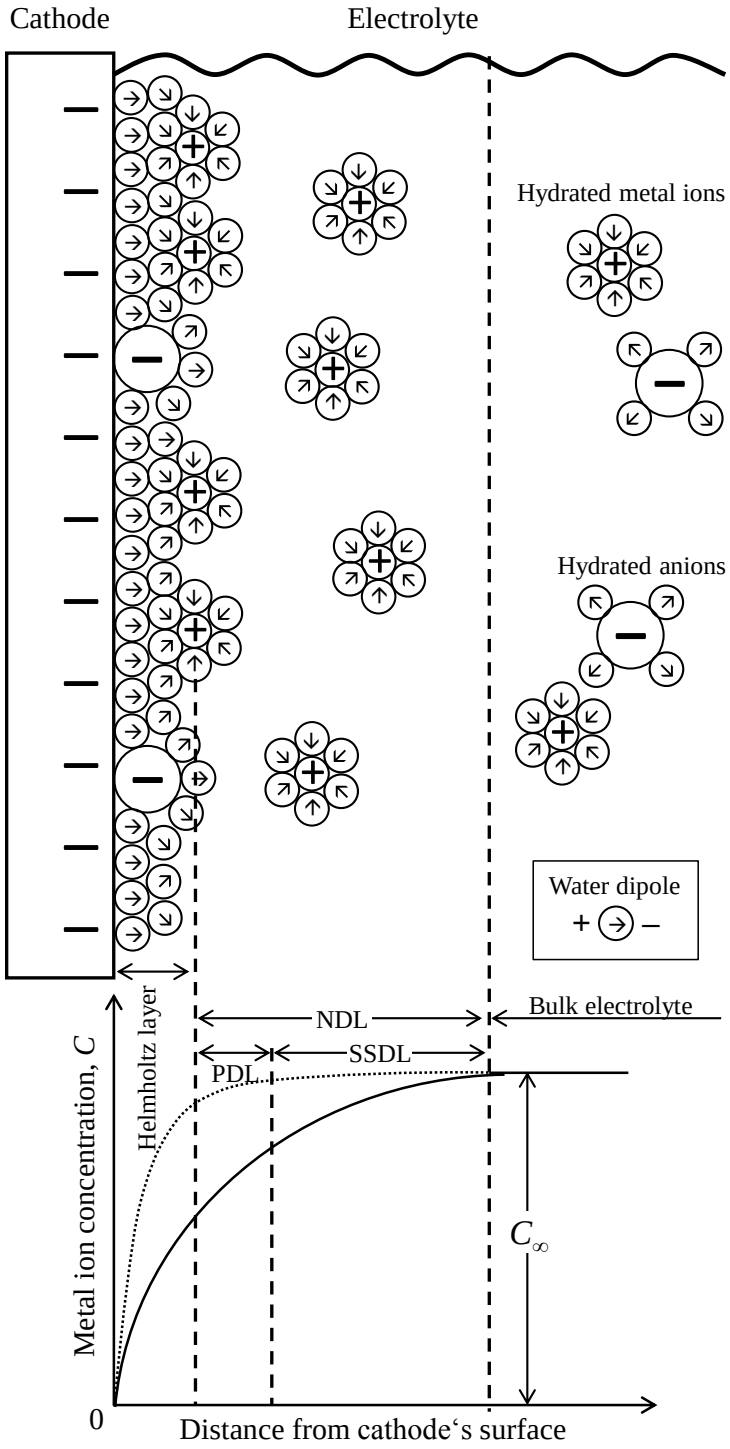

Figure 2.9: Electrostatically adsorbed water dipoles and specifically adsorbed anions based on the Sterm-Graham model. A Helmholtz layer consists of an adsorbed layer of water molecules, certain surface-active species, and adsorbed metal ions (*top*) [92]. A metal ion concentration over a distance from the cathode's surface, where NDL, PDL, and quasi-steady-state (SSDL) diffusion layers are built up under DC and pulse plating (*bottom*). The permission to reuse and modify the figure has been granted by Elsevier Books under a license 3713690979625.

but at the same time, it is used for establishing other chemical reactions. For example, three cathodic reactions occur in Cu electroplating using a cupric nitrate solution in a diluted nitric acid: the deposition of Cu (the reduction of cupric ions) and the reduction of both nitrate and hydrogen ions. The ratio between W_a [g] and W_T [g] is defined as a cathode efficiency $a_{\text{eff.}}$ [93].

$$a_{\text{eff.}} = \frac{W_a}{W_T} \tag{2.4}$$

In the DC plating, a complex geometry and a pronounced surface morphology of a specimen are two main factors that are causing an unevenly distributed coating thickness. Geometric factors illustrated in Figure 2.10(a), such as size and shape of the specimen and the arrangement of an anode and a cathode, could lead to the non-uniformity in local current densities generating a non-uniform electric field between the anode and the cathode. A high electric field will be generated between the anode and a local specimen's part which is close to the anode, and forces more coating ions to move towards this part in contrast to the other part, which is farther from the anode. Moreover, before the coating ions reach the cathode's surface, they have to diffuse through NDL. If this layer is thicker than a surface roughness or other protrusions as shown in Figure 2.10(b), then the coating ions will diffuse preferably with a shorter distance to reach these peaks rather than the distance for reaching other surface morphologies, which are below the roughness' peaks or the protrusion's peaks. Metals are thereby favorable to be deposited at these peaks, where the deposit thickness will be greater than in the surrounding surface. As a consequence, the roughness will become more pronounced after electroplating [92].

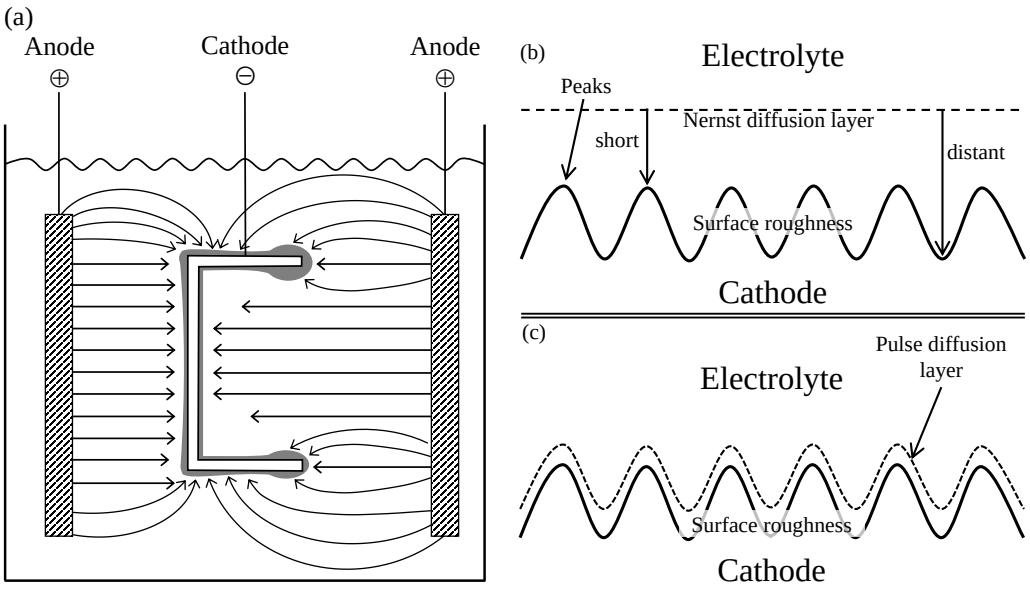

Figure 2.10: Electroplating of a specimen having a complex geometry (a) and a pronounced surface morphology using a DC (b) and a pulsed (c) current. Arrows in (a) represents the electric fields, which are not uniform on the exposed specimen's surface. The permission to reuse and modify the figure has been granted by Elsevier Books under a license 3713691041800.

The role of pulse plating is to modify NDL so that all the incoming ions diffuse in the same distance over surface morphology as shown in Figure 2.10(c). In the previous work, the thickness non-uniformity of Ni structures, electroplated using a constant electric current (DC plating) and a small volume of electrolyte, over a wafer was above 10 % [94], which could

lead to the separation between Ni-Sn structures on the top wafer and on the bottom wafer even though bond pressure is applied. For these reasons, the pulse plating is developed to overcome this problem.

Improvement in the layer properties

In pulse plating, an electric pulse can be generated by setting the ON time (t_{ON}) and OFF time (t_{OFF}) duration as depicted in Figure 2.11-*middle*. As schematically shown in Figure 2.12, the metal ion concentration at the cathode's surface decreases, during the first t_{ON}, and then increases during t_{OFF}, and once again decreases during the second t_{ON}, increasing again in the second t_{OFF} and so on. Thus, in this quasi-steady-state, a metal ion concentration on the cathode's surface is significantly higher than in the DC plating. Beside metal ions, other species, both anions or organic molecules, can diffuse into the bulk electrolyte during t_{OFF}. As shown also, the concentration of the anions increases at the end of first t_{ON}, and then decreases during t_{OFF}, and so on. This progressive decrease continues until the quasi-steady-state is reached, the value being significantly lower than in the DC plating. Therefore, the probability of such contaminants being incorporated into an electroplated layer, is reduced and the purity of pulse-deposited layers are usually higher than of DC-deposited layers.

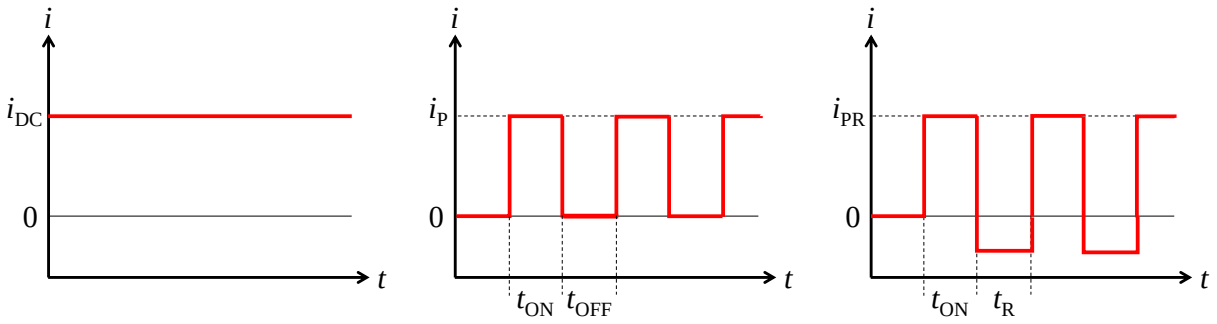

Figure 2.11: Sketch of DC current (*left*) and pulses as a function between current and time; without (*middle*) and with (*right*) reverse current (i_{PR}).

During t_{ON}, a DC current flows and therefore NDL is built up. During t_{OFF}, the electric field vanishes causing NDL collapses. This layer is built up and collapses in synchronism with the

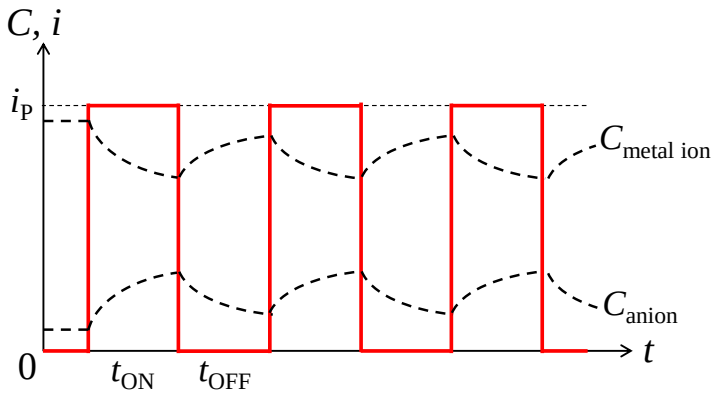

Figure 2.12: Concentrations of metal ions and anions during a pulse plating [92]. The permission to reuse and modify the figure has been granted by Elsevier Books under a license 3713691041800.

pulse frequency, and the concentration of metal ions within NDL follows the pulse as well. The repetition of this cycle of the NDL formation and the NDL collapse with the corresponding change in metal ion concentration will reach the quasi-steady-state, where NDL is improved significantly. The NDL is divided into two layers, namely pulse diffusion layer (PDL) and steady state diffusion layer as illustrated in Figure 2.9-*bottom*. The thickness of PDL is typically lower than the peaks of the surface roughness or of the protrusions (see Figure 2.10(c)).

In a specific application, t_{ON} with a reverse current (negative electric current) can be included as well as depicted in Figure 2.11-*right*. Usually, the reverse current is applied to replenish the recesses deposited on the tips or on the edges of specimen. As a consequence, the non-uniformity of a deposit thickness can be minimized and meanwhile the deposition rate can be enhanced. In order to increase the number of sites where the metal can be deposited and to improve the adhesion of the electroplated layer, a high current density could be applied at the beginning of the pulsed current for enhancing the cleaning action, presumably by a cathodic desorption, by creating a strong reducing environment at the cathode's surface. In addition, the increased current density is thought to increase the free energy of the charge carriers, so that the number of nucleation increases. The pulse plated layer therefore tends to be more fine-grained and denser (less porous) and better adhering than the DC plated layer [92].

Electroplated Ni and Sn layers

If a pulse consists of t_{ON} and t_{OFF}, then the duration of electroplating time is modified by the ratio between t_{ON} and the sum of t_{ON} and t_{OFF}, namely the duty cycle dc. In Equation 2.3, W is W_T and the proportionality constant M/nF for Ni and Sn electroplating equals 1.095 and 2.215, respectively. Here, the Faraday's constant F equals 26.799 A h. If W_T in Equation 2.4 is substituted with the one in Equation 2.3, then the cathode efficiency $a_{\text{eff.}}$ for the pulse plating can be derived as

$$a_{\text{eff.}}(\text{Ni}) = \frac{W_a}{1.095\, I\, dc\, t} \tag{2.5}$$

for Ni electroplating and

$$a_{\text{eff.}}(\text{Sn}) = \frac{W_a}{2.215\, I\, dc\, t} \tag{2.6}$$

for Sn electroplating.

A wafer having a plating base on the wafer's front side may be used as a cathode for electroplating. Generally, an electric current source is contacted at the wafer's edge. As the electric current flows, a potential drop is generated starting from the contact to the wafer's center due to the sheet resistance of the plating base. Consequently, the current density at the wafer's center is lower than at the wafer's edge (a geometric factor). For Ni electroplating, this difference of current density can influence the thickness uniformity of the electroplated Ni structures so that a Ni structure on the wafer's center is thinner than on the wafer's edge. A Ni electrolyte can be made from a sulphamate bath, in which an insoluble anode can be employed. The internal stress of a Ni layer, electroplated using this type of bath, is typically 0–55 MPa (tensile stress) [93]. However, this internal stress increases if the Ni layer is annealed to an elevated temperature, as depicted in Figure 2.13, which could cause layer delamination.

A Sn structure can be electroplated using an insoluble anode if an alkane sulfonate bath is employed. For environmental reasons, it is favorable to deposit a lead-free Sn structure. An electroplated Sn structure usually exhibits a large grain size and thus high surface roughness, which are not favored in microelectronic applications. Therefore, in Sn electroplating, it is more

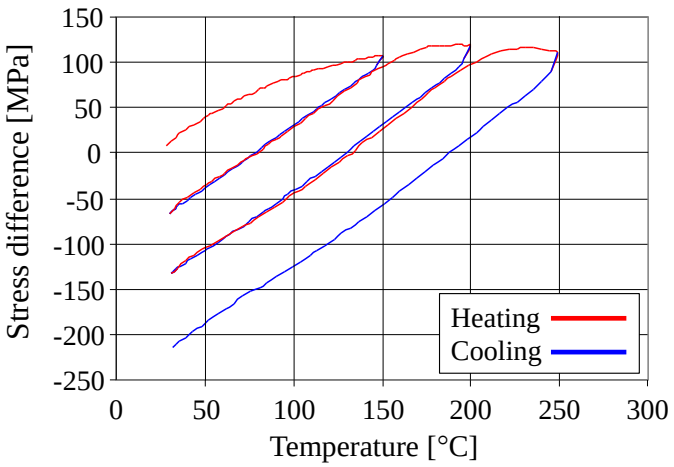

Figure 2.13: Internal stress evolution of an electroplated Ni layer during thermal cycling test. The stress increases up to 100 °C annealing and decreases to a stress below the initial stress after cooling down to RT. After three cycles, the stress decreases even lower [95].

in demand to develop a fine-grained Sn structure rather than to investigate the structure thickness uniformity. Due to a surface roughness, electroplated Sn structures can have the appearance of bright, satin bright, and matte. It was reported that the application of a pulse plating changes the surface morphology of the Sn structure significantly from a columnar-type microstructure to a well-polygonized, large-grained microstructure [93].

Electroplated Ni structures using a high current density exhibited a high tensile stress, a low elastic modulus, and a rabbit-ears-like shape profile of the cross-sectional Ni structure. While using low current density, the layer exhibited a compressive stress, a high elastic modulus, and a cap-like shape profile [96, 97]. On the other hand, a pulse-plated Ni structures using a high current density exhibited a low tensile stress but a high yield and a tensile strength as well as a high hardness due to a grain refinement [98, 99]. The crystalline orientation of the pulse-plated Ni structure was only influenced by the applied current density and t_{ON} [100]. The pulse plating combined with a reverse current could deposit a 1-mm-thick stress-free Ni coating for a good corrosion protection [101]. The application of a reverse current in the pulse plating could also modify a crystalline orientation and a surface roughness as well as a hardness of electroplated Ni structures by adjusting the duty cycle [102–104]. A pulse plating with a reverse current was performed to deposit a uniform Ni structure thickness for fabricating a circular grating consisting of several hundreds of concentric zones with a radially decreasing zone width [105]. Here, the pulse plating was employed to deposit NiFe alloy in fabricating a micro coil, a micro channel, and a micro switch [106, 107]. A pulse-plated NiFe alloy was deposited successfully in the fabrication of a magnetic microstructure [108, 109].

2.3 Transfer length method (TLM)

In the semiconductor technology, junctions are made between *n*-type and *p*-type semiconducting layers in order to fabricate, for example, a bipolar transistor. These semiconducting layers are normally contacted with a metal for establishing the electric current so that a transistor can be operated. The current, which is flowing through the interface between a metal and a semiconducting layer, encounters an electrical resistance, namely contact resistance R_C. It is also

useful to define a contact resistivity ρ_C, which equals to R_C/A, where A is the effective contact size, because it determines the resistance independently from the contact area size. Therefore, it is a convenient parameter while comparing contacts of different sizes.

In order to measure ρ_C, generally TLM is applied. The method is based on the reachable distance, namely transfer length L_T, where the current can enter a contact metal from a semiconducting layer or enter a semiconducting layer from a contact metal. As depicted in Figure 2.14, L_T is occurred because the current flow encounters the sheet resistance R_{sh} of the semiconducting layer and ρ_C. In order to determine these two parameters, a "ladder" structure, namely the TLM structure, of deposited contact metals on a semiconducting layer was proposed for determining R_{sh} as well as ρ_C [110, 111].

A TLM structure can be improved by depositing "ladder steps" unequally, in which the gaps

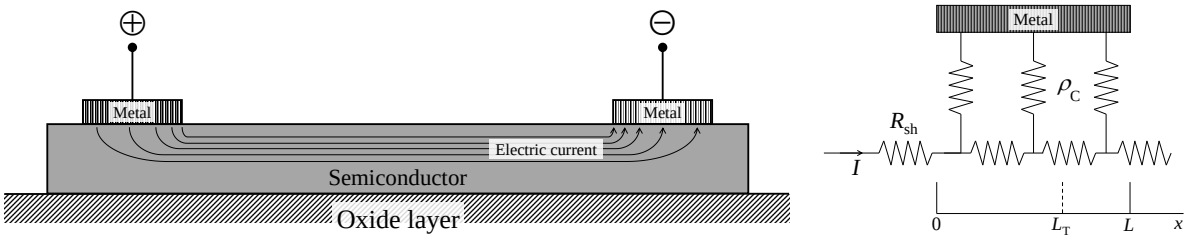

Figure 2.14: Transfer length principle. The voltage measured from x=0 to x=L is exponentially-like decreased.

between contact metals are unequal. With this form of a TLM structure, a voltage measurement, *i.e.*, electrical resistance measurement R_M, between two adjacent metals, namely TLM pads, can be performed without any perturbation from the other TLM pads in-between. This improved "ladder" structure is illustrated in Figure 2.15-*top*. If R_M is plotted against TLM gaps g and $L \geq 1.5\,L_T$, then a relation shown in Equation 2.7 can be applied to determine R_{sh} as well as ρ_C [110].

Equation 2.7 is extracted from a line, which is fitted linearly from the plots of R_M against g as depicted in Figure 2.15-*bottom*. R_{sh} can be determined from the slope of the fitting line, which equals to R_{sh}/Z. L_T can be determined as the line is extrapolated to g-axis where the coincidence point at this axis equals to $2L_T$. Lastly, ρ_C can be determined from Equation 2.8.

$$R_M = \frac{R_{sh}\,g}{Z} + 2R_C \approx \frac{R_{sh}}{Z}(2L_T + g) \tag{2.7}$$

$$\rho_C = R_{sh}\,{L_T}^2 \tag{2.8}$$

Factors, which influence the contact resistance, are the interfacial resistance generated within the interface between the semiconducting layer and the metal. It could also be from a portion of the metal immediately above that interface, a part of the semiconductor below that interface, current crowding effects, and any interfacial oxide or other layers that may be present between the metal and the semiconductor [110].

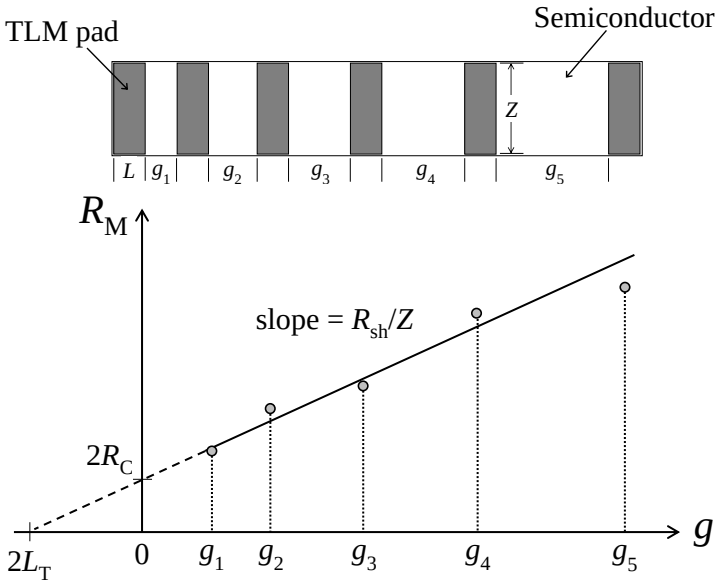

Figure 2.15: Schematic top view of TLM structure with unequally TLM gaps, (*top*). Schematic sketch of plots between R_M against g (*bottom*).

Chapter 3

Fabrication and characterization methods

3.1 Fabrication process

3.1.1 Diffusion barrier fabrication

The barrier fabrication was performed at the clean room of Fraunhofer Institute for Silicon Technology in Itzehoe, Germany (FhG-ISiT). Two types of *c*-Si wafers with 200 mm of diameter (8"-wafer) were used. The first type was a standard 8"-wafer without an oxide layer and the second type was a standard 8"-wafer with a ~4-µm-thick poly-Si layer. Prior to the poly-Si layer deposition, a 1-µm-thick thermal Si oxide layer was grown on the wafers. After the poly-Si layer deposition, chemical-mechanical polishing was performed on the wafer's front side in order to have a planar surface with a very low roughness. The barriers were deposited in a form of stacking layers using two PVD methods, *i.e.*, sputter deposition and evaporation, based on their availability in the production tools.

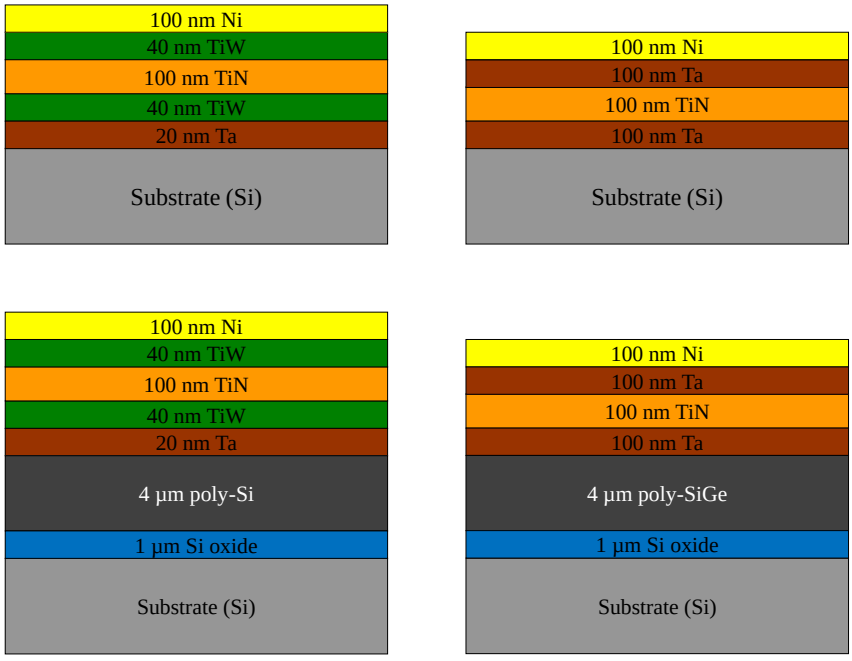

Figure 3.1: Cross-sectional sketches of the TiW-based (*left*), and Ta-based (*right*) barriers. The thicknesses of the stacking layers are also indicated.

Based on chapter 2, two types of barriers (TiW-based and Ta-based) were fabricated. To deposit the stacking layers of the TiW-based barrier, first a Ta layer was deposited by the evaporation without pre-etching a native oxide on the wafer's surface. After that, the wafer was transferred from the evaporator into the sputter chambers (a vacuum break) for depositing the TiW, TiN, and TiW layers sequentially with pre-etching a native oxide on the Ta layer's surface. After that, the wafer was transferred back from the sputter into the evaporator chambers (a vacuum break) for depositing a Ni layer without pre-etching. To deposit the stacking layers of the Ta-based barrier, first a Ta layer was deposited by the evaporation without pre-etching an native oxide on the wafer's surface. After that, the wafer was transferred from the evaporator into the sputter chambers (a vacuum break) for depositing a TiN layer with pre-etching an native oxide on the Ta layer's surface. After that, the wafer was transferred back from the sputter into the evaporator chambers (a vacuum break) for depositing Ta and Ni layers sequentially without pre-etching. Figure 3.1 illustrates the cross-sectional sketches of both barriers. This procedure was also performed for the barrier deposition on poly-Si and poly-SiGe layers for the $T_{10}W_{90}$-based and Ta-based barriers, respectively. The poly-SiGe layer was used because, as a thermoelectric element operated efficiently at high temperatures, it is also necessary to investigate the reliability of the barrier deposited on such layer. After barrier deposition, the wafer was diced into chips of $1 \times 1\,\mathrm{cm}^2$ size.

Prior to the barrier deposition, the wafers were cleaned wet-chemically to remove organic and inorganic contaminations. The cleaning was performed in three steps, which were distinguished from the type of the chemical solution, inside a designated tool (Spray Acid Tool, Semitool GmbH). Table 3.1 lists the cleaning steps.

Table 3.1: Wet chemical cleaning

Steps	Solutions and Composition	Temperature	Duration	Contaminant removal
1	$H_2SO_4 : H_2O_2 = 12 : 1$	110 °C	3 min	Organics
2	$H_2O : NH_4OH : H_2O_2 = 10 : 2 : 1$	60 °C	3 min	Organic, some metals, particles
3	$H_2O : HCl : H_2O_2 = 25 : 1 : 1$	80 °C	1 min	Remaining trace of metals

3.1.2 Bond solder fabrication

Bond solder fabrication was performed partly inside the clean room (Kiel NanoLab) of the Christian-Albrechts-Universität in Kiel, Germany. A *c*-Si wafer with 150 mm of diameter (6"-wafer) and a 1.5-µm-thick Si oxide layer on the front and back sides was used. The fabrication process is shown schematically in Figure 3.2 and its steps are following:

1. Wet chemical cleaning of two wafers using the procedure described in Table 3.1,
2. Lithography on the wafer's back side for both wafers to create a photoresist mask for the oxide etching,
3. Oxide dry etching to create a hard mask for the Si etching followed with stripping the photoresist,
4. Si wet etching to create bond and dicing mark structures followed with wet chemical cleaning procedure described in Table 3.1,
5. The TiW-based and Ta-based barrier deposition with a Ni top layer as the plating base,
6. Lithography on the wafer's front side for both wafers to create a photoresist pattern for electroplating followed with O_2 plasma etching to clean the plating base from a not-developed photoresist,

7. Electroplating the Ni and Sn structures (see chapter 3.2.3) sequentially followed with stripping the photoresist. Prior to the electroplating, both wafers were immersed in a HAc (acetic acid) solution to remove the native oxide on the surface of the Ni layer,
8. Lithography on the wafer's front side for both wafers to create a photoresist mask for protecting the electroplated Ni-Sn structures from ion beam etching,
9. Ion beam etching to structure the barrier followed with stripping the photoresist using acetone, isopropanol, and distillated water in a spin etcher,
10. Wafer alignment by aligning two bond marks (made from electroplated Ni-Sn structures) on the front side of a wafer with two bond marks on the back side of the other wafer. If necessary, both wafers were immersed in the HAc solution to remove the native oxide on the Sn surface, prior to the wafer alignment,
11. Wafer bonding using a customized recipe, and
12. Wafer dicing to obtain a number of a single dice for the solder contact characterization.

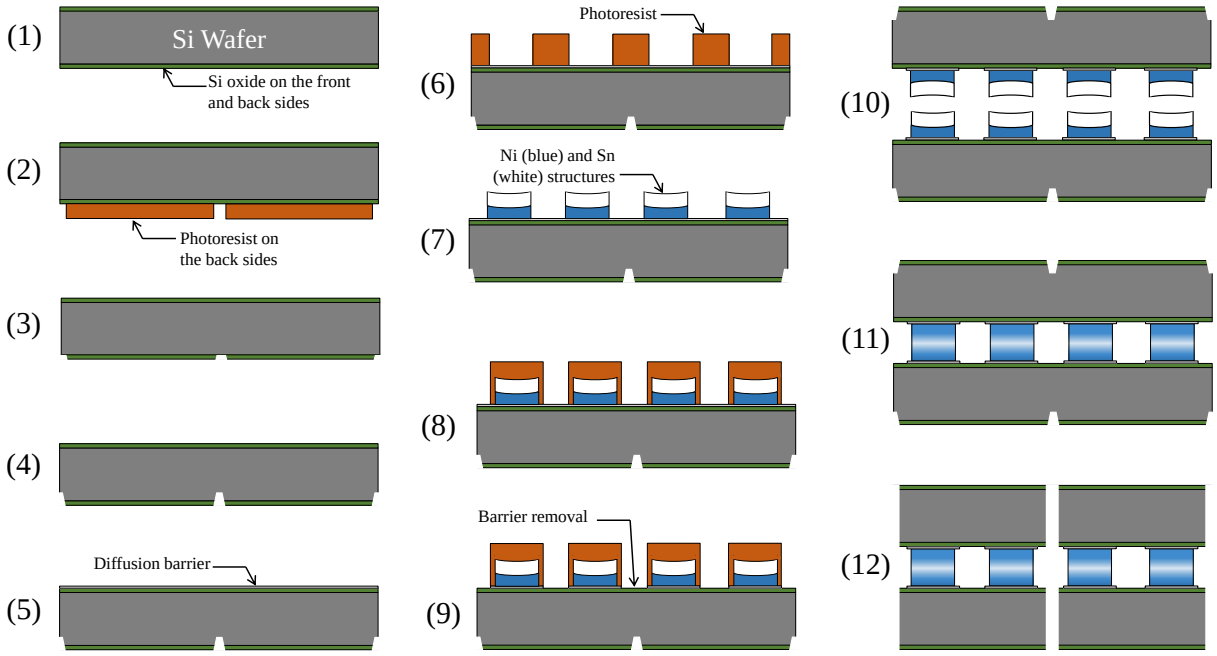

Figure 3.2: Cross-sectional sketch of the process steps of the solder contact fabrication. Description of the steps can be found in the text above.

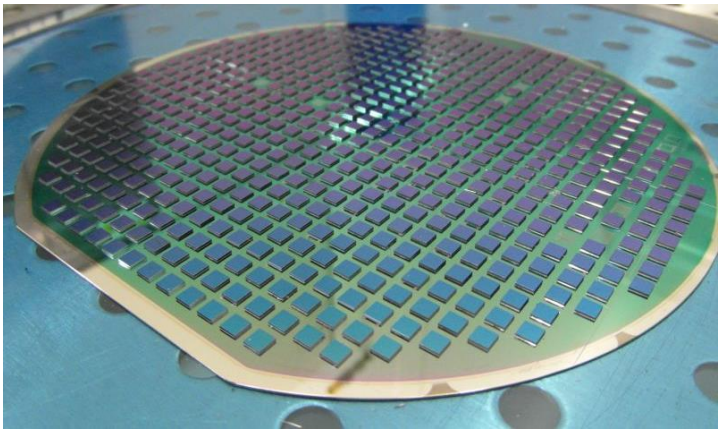

Figure 3.3: A bonded wafer after CAP dicing.

3.1.3 TLM structure fabrication

Transmission line measurement structure fabrication was performed partly inside the clean room (Kiel NanoLab) of the Christian-Albrechts-Universität in Kiel, Germany. The fabrication process is shown schematically in Figure 3.4 and its steps are following:

1. Four 8"-wafers of the second type (see chapter 3.1.1) were first prepared,
2. Lithography on the wafer's front side for all wafers to create a photoresist mask for structuring the poly-Si layer,
3. Reactive ion etching (RIE) to etch poly-Si layer anisotropically down to a few nanometer before oxide layer followed with stripping the photoresist,
4. RIE to remove necking and the thin poly-Si layer completely produced by first RIE followed with wet chemical cleaning in Table 3.1,
5. Barrier deposition; the TiW-based barrier on two wafers and the Ta-based barrier on the other two wafers, according to chapter 3.1.1,
6. (a) Lithography on two wafers having the TiW-based and Ta-based barriers to create a photoresist pattern for electroplating the TLM and contact pads. (b) Lithography using the pho-

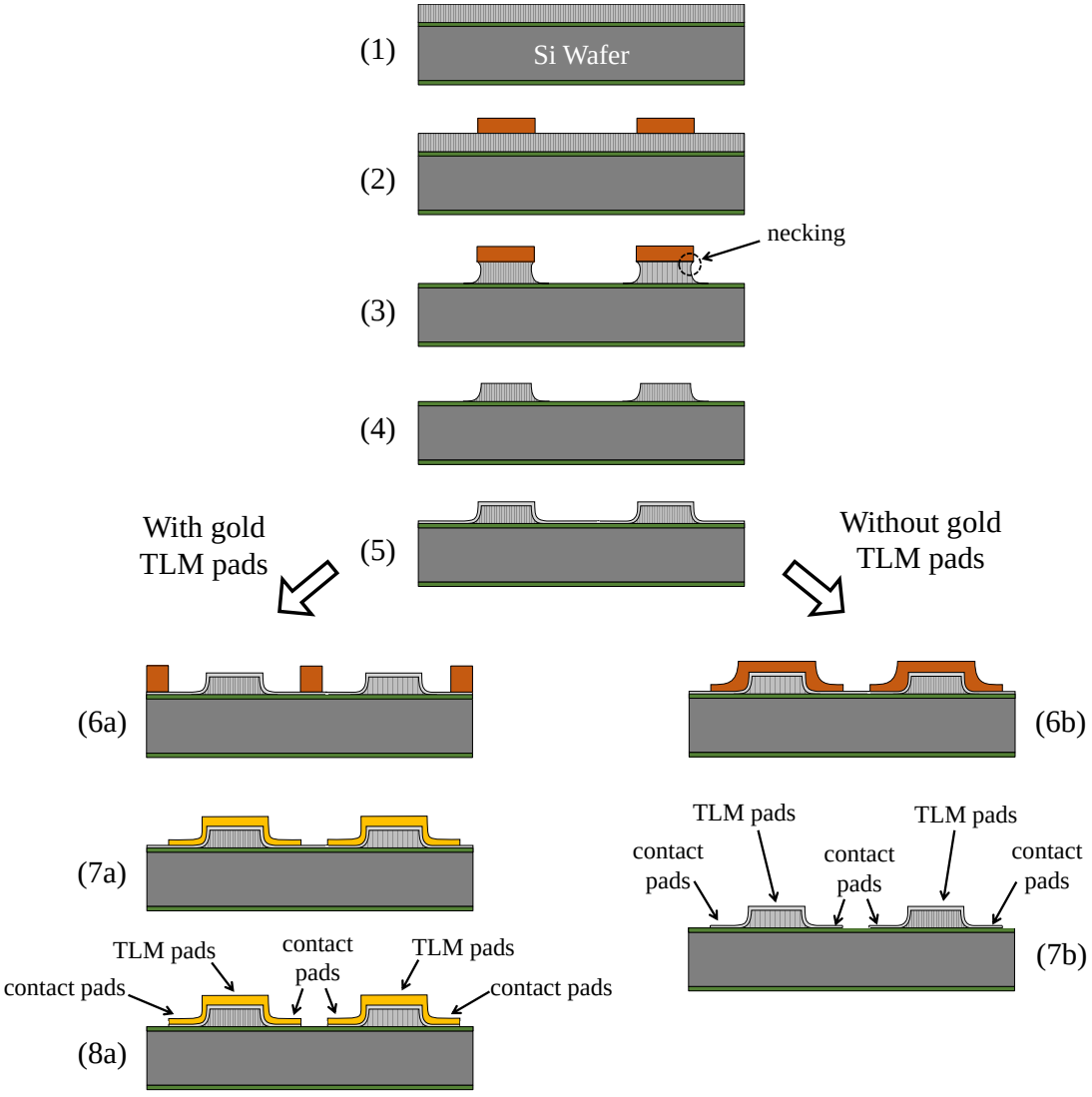

Figure 3.4: Cross-sectional sketch of the process steps of the TLM structure fabrication.

tomask for electroplating and an image reversal photoresist on the other two wafers having the TiW-based and Ta-based barriers to create a photoresist mask,

7. (a) Au electroplating followed with stripping the photoresist. (b) Ion beam etching to remove the exposed barrier completely,
8. (a) Ion beam etching to remove the exposed barrier completely.

After dry etching, the wafers were cut onto 26 reticles with $1.6 \times 1.50\,\mathrm{mm}^2$ of size. A reticle consists of 60 TLM structures. Figure 3.5 shows a fabricated TLM structure of a TLM reticle.

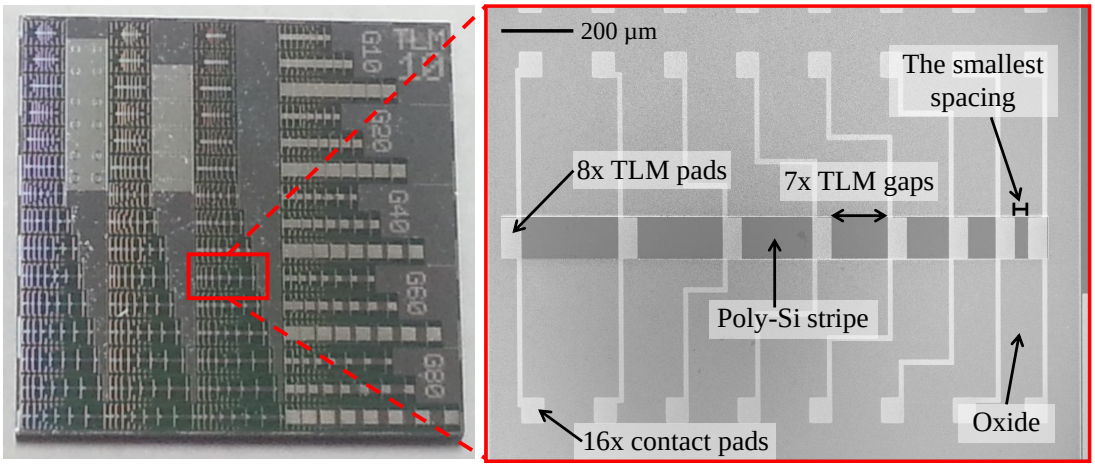

Figure 3.5: Top view of a fabricated TLM structure (*right*) magnified from a TLM reticle (*left*).

3.2 Fabrication methods

3.2.1 Physical vapor deposition

Two PVD methods, which were employed in the barrier fabrication, were sputter deposition (Oerlikon EVO LLS II) and evaporation (Balzers BAK760). The barrier consisted of stacked layers, which were deposited using a combination between both methods. This combination required a wafer transfer from the sputter to the evaporator chambers, and vice versa, that the wafer must had been exposed into air (vacuum break) consequently. Table 3.2 shows the thin layer materials and their deposition parameters, which were applied in both methods. In the

Table 3.2: Thin layer materials and their deposition parameters.

Paramater	Sputter depsosition			Evaporation	
	Ti	TiW	TiN	Ni	Ta
Base pressure [mbar]	1.0E-7	1.0E-7	1.0E-7	1.0E-7	1.0E-7
Distance between target and substrate [mm]	~130	~60	~130	~65	~65
Source power [kW]	4 DC	1.5 DC	2 DC / 1 RF	-	-
Temperature [°C]	RT	RT	RT	RT	RT
Ar flow [sccm]	70	80	55	-	-
Purity of targets [%]	99.995	99.99	(see Ti)	-	-
Operating pressure [mbar]	3.0E-3	5.6E-3	2.8E-3	2.2E-6	7.0E-6
Power [%]	-	-	-	~31	~39
N_2 flow [sccm]	-	-	9	-	-

sputter deposition, pre-etching with ~35 Å/min of etch rate was always performed subsequently before the deposition in order to remove the native oxide on the wafer's surface. The pre-etch parameters were 5×10^{-7} mbar of a base pressure, 700 W of an RF source power, 12 sccm of an argon (Ar) gas flow, and 6×10^{-4} mbar of an operating pressure.

3.2.2 Lithography

Lithography masks

A transparent foil mask (KOENEN GmbH) with a high layout resolution (25,000 dpi) was used in the lithography for etching the oxide layer on the wafer's back side. Three Cr-glass photomasks (Compugraphics-Jena GmbH, 10 µm of minimal structure width) were used in the lithography. Two photomasks each for electroplating the Ni-Sn structures and for etching the barrier have an identical mirrored layout between the half-left and the half-right parts of the layout. Therefore, only a photomask required to perform a lithography (for electroplating the Ni as well as the Sn layers) on two wafers, which will be bonded. However, the daisy chain layouts have a contact pads design only on the half-left part of photomask's layout. The photomask for etching the barrier has a similar layout with the photomask for electroplating the Ni-Sn structures but the layout is enlarged 1.4 times. The photomask for TLM structure fabrication has a layout, which is divided into two part; on the half-top part is the layout for etching the barrier and on the half-bottom part is the layout for structuring the poly-Si layer. Therefore, the photomask can be used in two lithography steps.

Bond alignment and dicing marks

The lithography steps are following:
1. Deposition of HMDS at 120 °C in the gas phase (Süss MicroTec ACS200).
2. Deposition of a 2-µm-thick photoresist (Fujifilm HiPR) using a spin coating method at 3000 rpm for 30 s (Süss MicroTec ACS200).
3. Sequentially, a soft bake of the photoresist at 90 °C for 60 s on a hot plate.
4. Exposure of a UV light with 140 mJ/cm^2 of a dose for 3 s (Süss MicroTec MA150) on the photoresist using the transparent foil mask and a hard contact method.
5. Post exposure bake of the UV-exposed photoresist at 110 °C for 60 s on a hot plate.
6. Development (Süss MicroTec ACS200) of the UV-exposed photoresist in a developer solution (Fujifilm OPD4262) for 60 s followed with rinsing and drying the wafer.
7. Hard bake of the developed photoresist at 120 °C for 60 s on a hot plate.

Ni-Sn electroplated structures

The lithography steps are following:
1. Wafer heating at 120 °C for 60 s on a hot plate to vaporize the remained water on the wafer surface.
2. After cooling down, deposition of a 10-µm-thick photoresist (MicroChemicals AZ4562) using spin coating method (OPTI spin ST22P) at 1850 rpm for 45 s.
3. Sequentially, soft bake of the photoresist at 120 °C for 4 min on a hot plate.
4. After cooling down, a manual EBR (Edge Bead Removal) of the photoresist ~2.5 mm from the wafer's edge. To perform this, the wafer is rotated at 800 rpm for 80 s while the acetone is sprayed on the wafer's edge using a 5-mL-volume syringe for a number of time.

5. Back side alignment between the photomask and the alignment marks on the wafer's back side prior to the UV exposure (Süss MicroTec MA6/BA6).
6. Exposure of a UV light with 1500 mJ/cm^2 of dose (Süss MicroTec MA6/BA6) on the photoresist using the Cr-glass photomask and a low vacuum contact method with 15 s of hold time.
7. Development of the UV-exposed photoresist in a dissolved developer, which contains of a mixture between a developer (MicroChemicals AZ400K) and the DI water with a ratio AZ400K:H_2O = 4:1. After an immersion for 2 min, the photoresist is rinsed with the DI water and then immersed again for another 2 min. This repetition must be performed continuously until the UV-exposed photoresist were completely etched.
8. After a successful development, the wafer is rinsed and dried using a spin dryer.

Etching the diffusion barrier and the poly-Si layer

The lithography steps are following:
1. Deposition of HMDS at 50 °C in the gas phase (OPTI spin ST22P).
2. Deposition of a 4.3-µm-thick photoresist (Fujifilm OiR908-35) using spin coating method at 2800 rpm for 30 s (OPTI spin ST22P).
3. Sequentially, soft bake of the photoresist at 90 °C for 60 s on a hot plate.
4. After cooling down, front side alignment between the photomask and the alignment marks on the wafer's front side (Süss MicroTec MA6/BA6).
5. Exposure of a UV light with 480 mJ/cm^2 of dose (Süss MicroTec MA6/BA6) on the photoresist using the glass-Cr mask and a low vacuum contact with 15 s of hold time.
6. Sequentially, post exposure bake of the photoresist at 90 °C for 60 s on a hot plate.
7. Development of the UV-exposed photoresist in a developer solution (Fujifilm OPD4262). After an immersion for 30 s, the photoresist is rinsed with DI water and then immersed again for another 30 s. This repetition must be performed continuously until the UV-exposed photoresist were completely etched.
8. After a successful development, the wafer is rinsed and dried using a spin dryer.

3.2.3 Electroplating of the Ni and Sn structures

Lab-scale electroplating tool

A lab-scale electroplating tool, which is depicted schematically in Figure 3.6, was designed and fabricated in order to provide the deposition of the Ni and Sn structures. The advantages of this tool are that it can uses a small amount of an electrolyte (up to 1.5 L), it has a feature of a wafer front side contact, and it can be applied to perform an electroplating either on a 6"- or an 8"-wafer. To enhance the thickness homogeneity of electroplated structures over a wafer, it uses a pulsed electrical current and a wafer rotation. The tool consists of following parts:
1. Metallic ($AlMg_3$) wafer holder. As seen schematically in Figure 3.7, it has two parts; the bottom part (Figure 3.9-*right* is used for mounting the wafer (cathode) and has a build-in ring for establishing an electrical contact to the wafer front side (see Figure 3.8), and the top part (Figure 3.9-*left* is used for pressing the mounted wafer by fixing screws, so that the plating base on the 2.5-mm-exposed wafer's edge touches completely onto the build-in ring surface. The outer surface of the bottom part is powder-coated that isolates the holder electrically. In order not to let the electrolyte flowing into the wafer's back side during electroplating, rubber o-ring seals are mounted in several trenches.

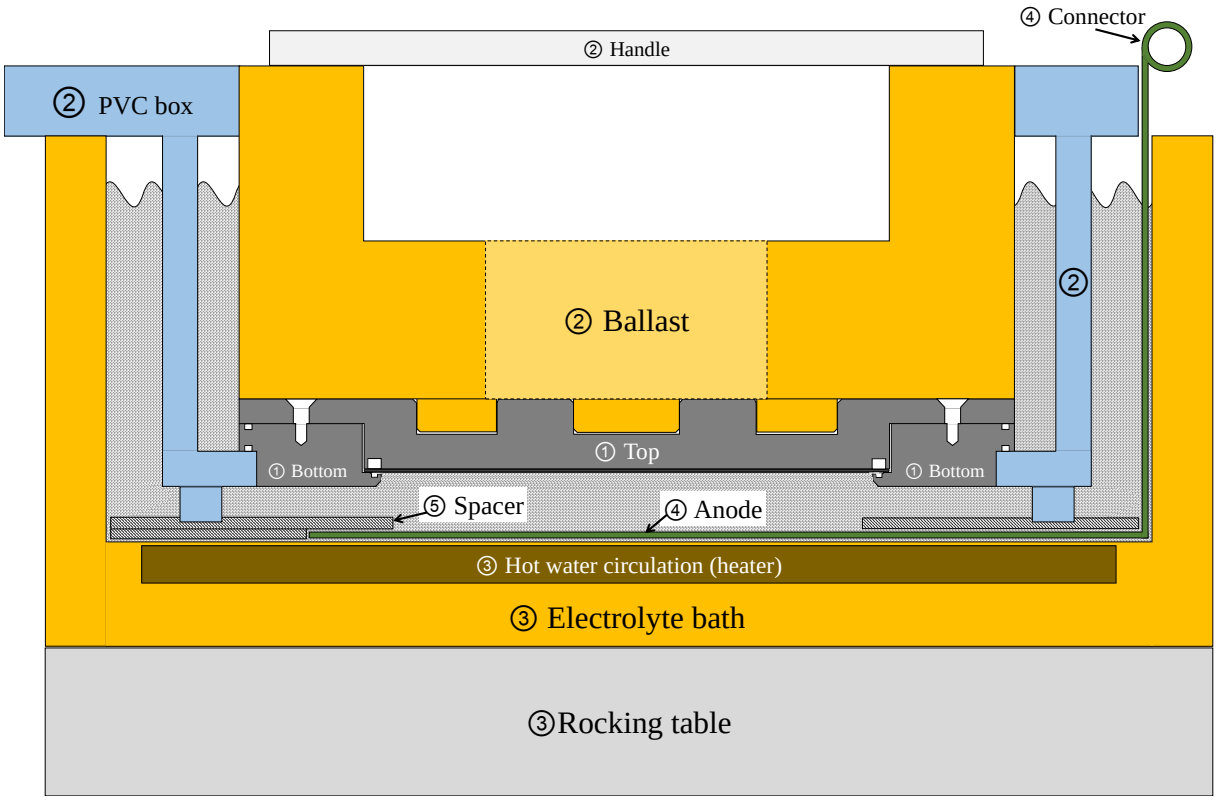

Figure 3.6: Cross-sectional sketch of a lab-scale electroplating tool.

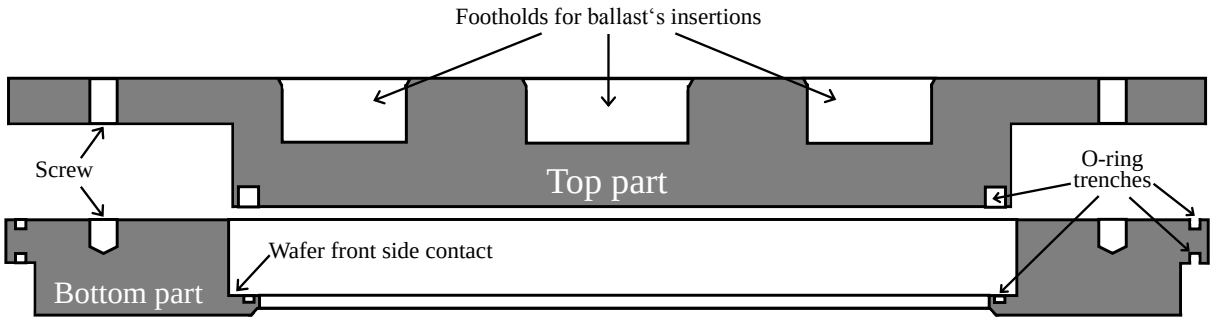

Figure 3.7: Cross-sectional sketch of the metallic wafer holder.

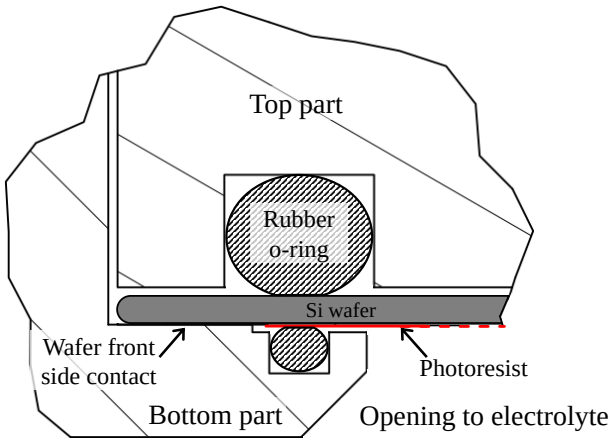

Figure 3.8: Schematic drawing of a cross-section of the wafer front side contact.

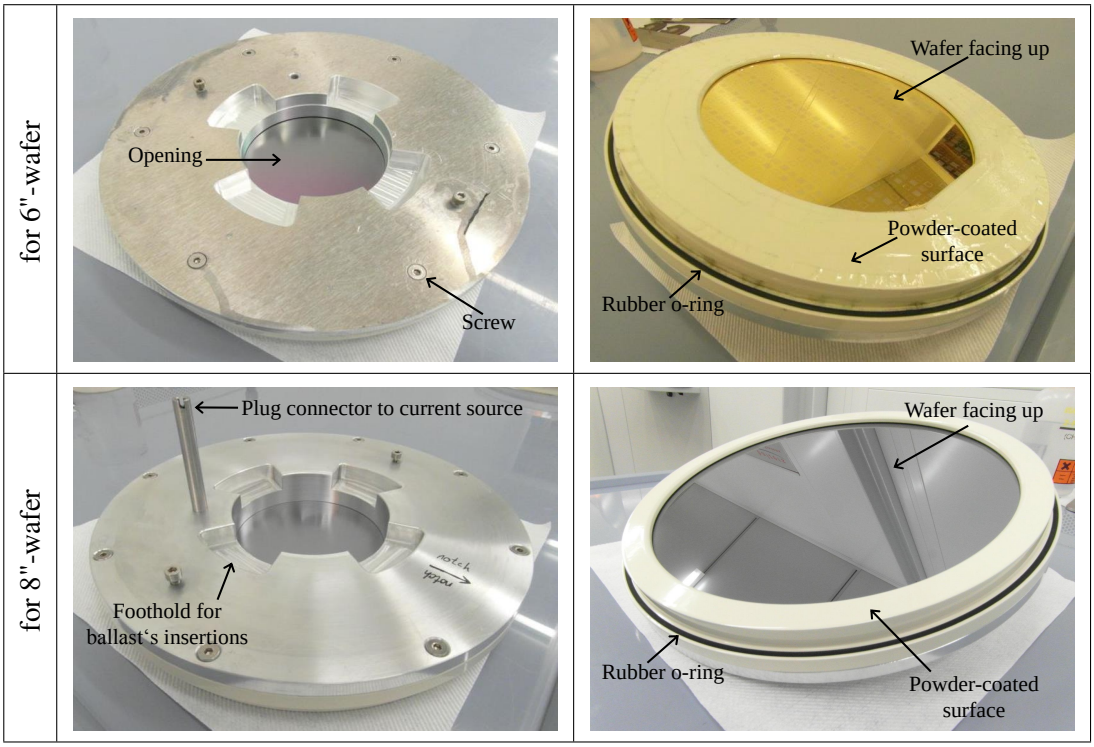

Figure 3.9: Metallic wafer holder for the electroplating on the 6"- and 8"-wafer.

2. PVC-made box with a rotary ballast. The metallic wafer holder is mounted inside a box and pressed down by a Teflon-made ballast, which can be rotated manually during electroplating.

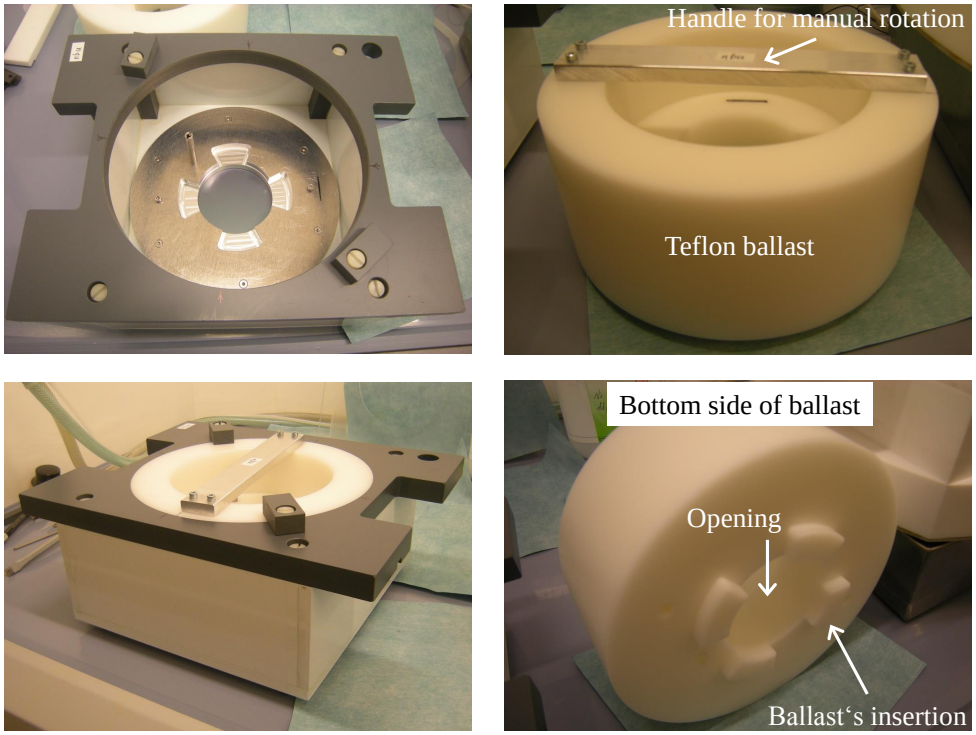

Figure 3.10: PVC-made box with its ballast.

3. Electrolyte bath ($270 \times 270 \times 114\,\mathrm{mm}^3$) made from Teflon with a rocking table. The bath is adequate up to 1.5 L of electrolyte. It has fluid channels beneath the surface's bottom to circulate hot water for heating the electrolyte.

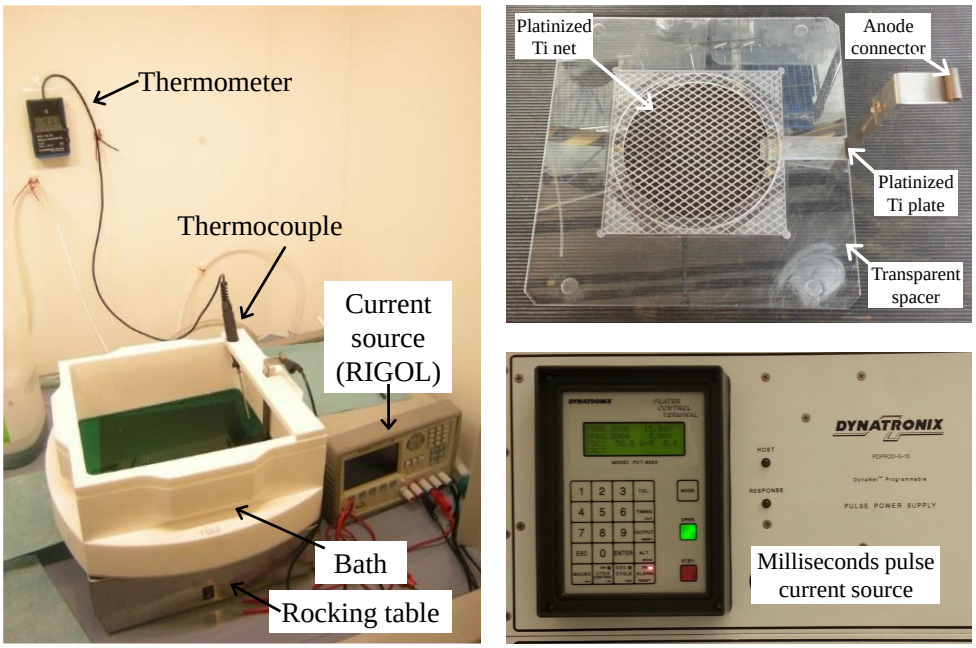

Figure 3.11: Electrolyte bath, thermometer, rocking table, anode, spacer, and current sources.

4. Platinized Ti anode. It has a net form with $160 \times 160\,\mathrm{mm}^2$ of size. A platinized Ti plate is welded on the net to provide an electrical connection from an electric current source to the anode.
5. Transparent spacer between the anode and the cathode. It is used for creating a circle area form of an electric current flowing from the anode to the cathode through the electrolyte, so that the exposed wafer surface received a homogeneous current density.
6. Electric current source. There were two types of source; the first type (RIGOL DP1116A) is capable to supply a DC and a 1-s-pulsed current, and the second type (Dynatronix PDPR 20-5-10) is capable to supply a millisecond-pulsed current.
7. A commercialized-available thermometer with a thermocouple.
8. Water conditioner (Julabo F25) for controlling electrolyte temperature by circulating temperature-regulated water through the fluid channels.

Ni and Sn electrolytes

To create an Ni or a Sn electrolyte, commercially-available solutions (Enthone GmbH) are mixed. The mixture of 1.5 L of an Ni electrolyte contains:

1. 648 mL of an Ni sulphamate (NICKELSULFAMATE SOLN 185G/L NI),
2. 18 mL of an addition agent C (LECTRO-NIC 10-03 ADD. AGENT),
3. 15 mL a wetting agent (LECTRO-NIC 10-03 WETTING AGENT),
4. 97.5 mL of an anode activator (LECTRO-NIC 10-03 ANODE ACTIV.),
5. 45 g of a boric acid (Carl Roth GmbH, ≥99.5 % Ph.Eur. USP BP), and
6. 50 mL of a dissolved sulphamic acid (Carl Roth GmbH, ≥99.5 % cryst.).

Preparation of 1.5 L of an Ni electrolyte is following:

1. Dissolve the boric acid powder in 200 mL of hot DI water,
2. Mix the dissolved boric acid into a hot Ni sulphamate,
3. While stirring, add sequentially the addition agent C, the wetting agent, and the anode activator into the solution no. 2,
4. Add DI water into the solution no. 3 up to 1.5 L of the total solution volume,
5. Determine the pH value of the solution in no. 4 using a color-fixed pH indicator strips (Macherey-Nagel GmbH pH-Fix 0.0-6.0), and
6. Reduce the pH value between 2.5 and 3.5 by adding the dissolved sulphamic acid piecemeal. The dissolved sulphamic acid was 20 g of the sulphamic acid powder mixed with 50 mL of hot DI water.

Tin electrolyte was based on an alkane sulfonate bath. The mixture of 1.5 L of a Sn electrolyte contains:

1. 99 mL of an Sn concentrate (STANNOSTAR A-300 TIN CONC.),
2. 150 mL of an acid concentrate (STANNOSTAR A-70 ACID CONC.), and
3. 60 mL of a smoothing agent (STANNOSTAR GMM SMOOTHING AGENT).

Preparation of 1.5 L of a Sn electrolyte is following:

1. Mix sequentially the acid concentrate and the smoothing agent into the Sn concentrate, and
2. Add DI water into the solution no. 1 up to 1.5 L of the total solution volume.

Pulse current electroplating (pulse plating method)

The Ni and Sn structures were deposited using a pulse plating method. Here, it will only be described the optimal electroplating procedure for a successful wafer bonding. However, the variety in the electroplating will be described in chapter 4.3.1 including its result.

Before the electroplating of the Ni and Sn structures, the wafer is treated in the O_2 plasma (see chapter 3.2.4 and immersed in 10 % of a HAc (Carl Roth GmbH, ROTIPURAN®100 % p.a.) solution (50 mL of 100 % HAc + 450 mL of DI water) for 10 min. Before immersion, the exposed plating base surface must be wet by spraying it with a high pressure of DI water (a DI water gun) in order to remove the air, which will cover the exposed plating base surface during immersion. After rinsing and drying, the wafer is mounted in the metallic wafer holder followed with the electroplating. Prior to mounting, the initial weight of the wafer having photoresist on the top is determined using a balance. After the electroplating, the wafer is dismounted, rinsed, and dried followed with the measurement of its final weight. The weight difference before and after electroplating is used to determine the cathode efficiency of the electroplating.

The Ni electroplating is performed at an electrolyte temperature between 35 °C and 40 °C. Therefore, it is necessary to set the bath temperature before performing the actual electroplating, otherwise the electrolyte temperature will drop significantly due to the metallic holder and PVC box, which have a cold body. To do this, a clean blank wafer is mounted (using the metallic holder and the PVC box and etc.) into the electrolyte without applying an electrical current. During the electrolyte agitation using the rocking table, the electrolyte is heated up to 40 °C. After the temperature is reached, then the blank wafer can be replaced with the actual wafer.

The procedure of the Ni electroplating is following. After mounting all parts in the Ni electrolyte bath, the cables from pulsed current source are plugged in to the cathode and the anode followed with switching on the rocking table. After few seconds, the pulsed current source is switched on. The source has a controller, which can be programmed to deliver a pulsed current with a specified t_{ON} and t_{OFF} in a milliseconds range and a specified i_P. In this work, the optimal program parameter for pulsed time is t_{ON} = 10 ms and t_{OFF} = 10 ms within

12 min of electroplating total time, and $i_P = 0.5\,A/dm^2$ for 1 min, $i_P = 1.5\,A/dm^2$ for 1 min, and $i_P = 3\,A/dm^2$ for 10 min (12 min in total). A wafer rotation is performed manually within 12 min by rotating the ballast with the help of a handle. The wafer is mounted with the wafer's flat facing to the anode plug connector and then the pulsed current source is switched on. The manual rotation has been performed in such a way to improve the thickness uniformity of the Ni structures over a wafer.

For the Sn electroplating, the optimal program parameter for pulsed time is $t_{ON} = 10$ ms and $t_{OFF} = 10$ ms within 9 min of electroplating total time, and $i_P = 1.5\,A/dm^2$. The electrolyte temperature is 19 °C. The wafer rotation is negligible.

3.2.4 Etching

Silicon oxide etching (Sentech SI500)

Before etching the oxide, a cleaning program is executed to clean organic contamination on the chamber's wall. Using a blank wafer, the program utilizes an ICP and an RF generator operated at 300 W and 100 W of an electrical power, respectively, and an O_2 gas flowed at 99 sccm for 5 min.

The Si oxide etching utilizes an ICP and an RF generator operated at 800 W and 120 W of an electrical power, respectively, and a CHF_3 gas flowed at 50 sccm. The etching lasts for ~20 min. During etching process, the wafer is cooled from the back side with He gas and chamber pressure is maintained from 0.09 mbar to 0.176 mbar. This etching was used to etch an Si oxide layer with 1.5 µm thickness on the wafer's back side in order to create a hard mask for the wet Si etching.

Wet Si etching

This etching was performed at the clean room of FhG-ISiT. It utilizes alkali solution with 30 % of a KOH concentration heated at 80 °C. This etching was used to etch the Si substrate for 10 min, *i.e.* to create the bond and dicing marks on the wafer's back side. Prior to the wet Si etching, a photoresist on the wafer's back side was stripped sequentially inside two dissolvent baths (the EKC830 [112] and RER500 [113] baths) using 100 W of a ultrasonic power followed with rinsing and drying the wafer.

O_2 plasma etching (Sentech SI100)

Initially, the chamber is evacuated. After the vacuum is reached, the chamber is flowed with the O_2 gas and this gas flow is set in such way that the chamber pressure increases up to 0.4 mbar. After 30 s, an RF plasma with 150 W of an electrical power is switched on for 4 min. This etching is performed to clean the exposed plating base surface from the un-developed photoresist during lithography and to make a hydrophilic surface of the exposed plating base surface as well.

Ion beam etching (OXFORD Instruments PC3000)

Before etching the barrier, a warming-up program is executed to warm up the tool. The program utilizes a neutralizer and an RF generator operated at 400 mA of an electrical current and an 1000 W of an electrical power, respectively, for 12 min. Argon gas is flowed into the neutralizer

and beam chambers at 5 sccm and 10 sccm, respectively.

The etching of the barrier utilizes a neutralizer and an RF generator operated at 400 mA of an electrical current and at 1000 W of an electrical power. Argon gas is flowed into the neutralizer and beam chambers at 5 sccm and 10 sccm, respectively. An electron beam operated at 350 mA of an electrical current, at 400 V of a voltage, and at 400 V of an acceleration voltage is utilized to generate the ions. During etching, and the wafer is rotated at 8 rpm and tilted 30° from the vertical position, and the chamber pressure is maintained at $\sim 2 \times 10^{-4}$ mbar.

Reactive ion etching (Sentech SI500) of the Si layer

To etch the poly-Si layer using a resist mask, an ICP and an RF generator operated at 600 W and 120 W of an electrical power, respectively. The Ar and SF_6 gasses are flowed at 150 sccm and 50 sccm, respectively, into the chamber. The etching lasts for 180 s. During etching process, the wafer is cooled from the back side with He gas and the chamber pressure is maintained at 0.09 mbar.

To etch the poly-Si layer without a resist mask, both generator powers are operated at the same electrical power and the SF_6 gas is flowed with the same flow, however, the Ar gas is flowed at 145 sccm. This etching lasts for 10 s.

3.2.5 TLP Wafer bonding

A TLP wafer bonding requires an RT as the initial temperature and a high heating rate of top and bottom electrodes [73]. Therefore, a bond program was created to provide these requirements. The profiles of electrode temperatures and a bond pressure during a wafer bonding are depicted in Figure 3.12.

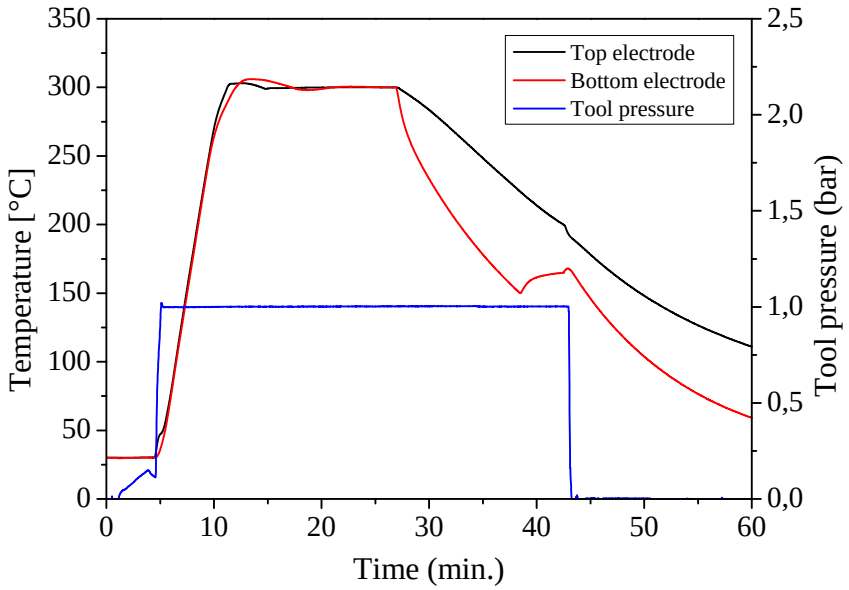

Figure 3.12: Temperature and pressure profiles during a TLP wafer bonding with 30 min of a bond time.

Initially, the temperature of the top and bottom electrodes is adjusted at 30 °C in the stand-by mode. After wafer alignment and inserting aligned wafer pair into the bond chamber, the bond program is started. The chamber is evacuated down to 5×10^{-5} mbar of pressure followed with

removing the fixture's spacers and then bringing down the top electrode. After this sequence, the tool pressure is increased gradually to a specified pressure, which is applied to the top electrode in order to press the wafer pair together followed with ramping up the temperature of both electrodes from 30 °C to 300 °C in 232 s. With this ramping, ~70 °C/min of a heating rate can be achieved with 4–7 °C of a temperature difference between the top and the bottom electrodes at the melting temperature of Sn. After both electrodes has reached 300 °C, the tool pressure and the electrode temperatures are maintained for a specified time. To retrieve the bonded wafer, the bond chamber is vented at an electrode temperature below 100 °C in order to avoid quenching. Table 3.3 lists the Ni-Sn TLP wafer bonding, which had been performed in this study using a commercially-available wafer bonder (Süss MicroTec SB6 and SB8).

Table 3.3: Parameters of the Ni-Sn TLP wafer bonding

Wafer bonding	Diffusion barrier	Bond time [min]	Bond pressure [bar]	Pressure on bond solder [MPa]	Average thickness of electroplated structures	
					Ni [µm]	Sn [µm]
wb-A	TiW/TiN/TiW/Ni	60	2.5	3.33	2.2	2.2
wb-B		60	4	5.33	4.8	2.6
wb-C	TiW-based	30	1	1.33	1.7	3.1
wb-D		15	2	2.66	4.5	3.5
wb-E		15	1	1.33	3.4	2.9
wb-F		15	0.5	0.67	2.5	2.5
wb-G	Ta-based	15	2	2.66	4.5	2.5
wb-H		15	1	1.33	2.4	2.5

3.2.6 Wafer dicing

The wafer dicing is performed (DISCO Automatic dicing saw DAD3350) in order to dice a bonded wafer so that desired dies, such as 16×16-array and daisy chain dies can be selected for the mechanical and electrical characterizations. Prior to dicing, a bonded wafer is mounted on the adherent side of a UV-curable dicing tape, which hold the bonded wafer on a metallic dicing frame. There are three steps to dice an Ni-Sn-TLP-bonded wafer. The first step is to cut the bonded wafer into half (the left and right sides), the second step is to dice the top wafer (a.k.a. CAP dicing), and the third step is to dice the bottom wafer (a.k.a. FINAL dicing). After performing the first step, the half-wafer side, where the daisy chain pads are facing down, is turned the up-side down (detached from the foil and then attached to a new foil). In the second step, the top half-wafer is cut into $3.5 \times 3.5\,\mathrm{mm}^2$ of size. In the third step, the bottom half-wafer is cut into $5 \times 4\,\mathrm{mm}^2$ of size. With this procedure, it is possible to obtain daisy chain dies in all locations from the Ni-Sn-TLP-bonded wafer.

3.3 Characterization methods

In order to investigate the reliability of barrier and Ni-Sn solder contact, eight characterization methods have been performed before and after annealing.

3.3.1 Annealing for the reliability investigation

The annealing was performed under vacuum (~3×10^{-6} mbar) at a specified temperature and for a specified duration. The specified duration of annealing was always 24 h for all specified temperatures. Except, for sheet resistance measurement, additional annealing for 3 and 7 days were performed. The specified annealing temperatures will be stated in the following sub-chapter of the characterization methods. The annealing setup consists of a vacuum pump (Pfeiffer Vacuum HiCube 80 Eco), a quartz tube as a chamber, a self-made stainless steel specimen holder, a K type (Ni-Cr) thermocouple, a temperature controller, and a furnace.

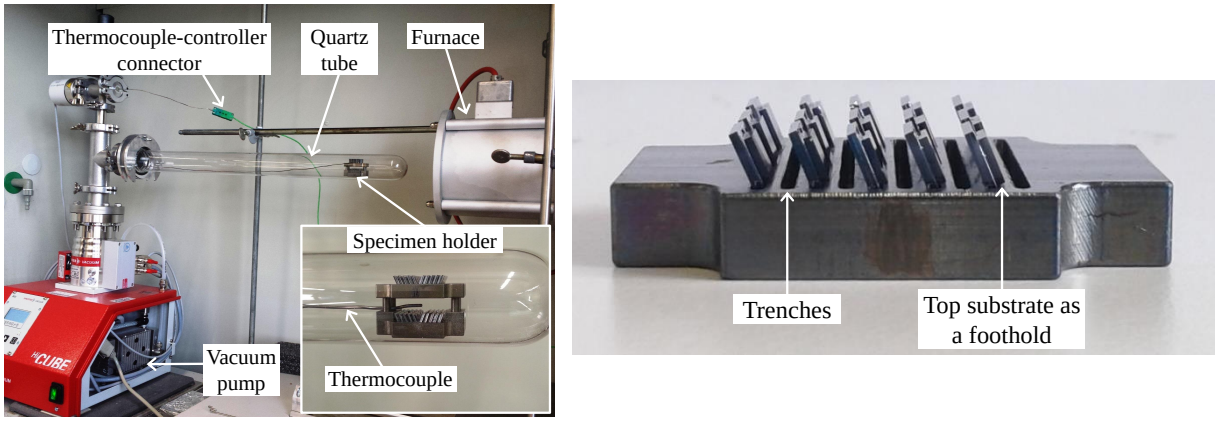

Figure 3.13: The annealing setup (*left*) and the specimen holder (*right*).

During annealing, the bonded dies is placed into trenches of the specimen holder, where the top substrate holds the die being drowned. This foothold can be an indicator that if the Ni-Sn bond solder is melted at 600 °C, then the top substrate must have detached or slid out from the bottom substrate. The thermocouple tip is positioned in the center of the specimen holder as shown in the inset in Figure 3.13, where the maximum and minimum differences of temperature at a die located away from tip are <5 °C. The thermocouple is connected to a temperature controller, so that the temperature on the specimen can be sensed and controlled at the same time. The furnace temperature is increased carefully using the controller, so that an overshooting from the desired temperature can be avoided.

3.3.2 X-ray diffraction analysis

The XRD analysis was performed using a Bragg-Brentano geometry (θ-2θ method) in an 4-axes X-ray diffractometer (SEIFERT XRD 3000PTS). The diffractometer operates at 40 V and 40 mA to generate a radiation from a Cu anode and utilizes an Ni filter to absorb the Cu-Kα radiation, so that an X-ray of Cu-Kα radiation with 1.540 Å of wavelength is used for the analysis. The incident X-ray beam (from source) is diverged by a slit with 2 mm of an aperture and the diffracted X-ray beam (to detector) is focused by a slit with 1 mm of an apertures. The diffraction was scanned from 25° to 65° of the 2θ angle with 0.05° of a step and 5 s of a hold time in order to find peaks, which satisfy the Bragg's law. Prior to the diffraction scan, all axes were calibrated to find the highest intensity of diffracted beam, which came to detector. This analysis had been performed on barrier dies, which were non-annealed (RT) and 24-h-annealed at 200 °C, 300 °C, 400 °C, 500 °C, 600 °C and 650 °C.

3.3.3 Transmission electron microscopy

Tool and sample preparation.

The TEM analysis was performed[1] using an FEI Tecnai F30 STwin microscope (300 kV, an FEG cathode, a spherical aberration coefficient C_s=1.2 mm). The chemical composition was determined using an EDX spectrometry (Si(Li) EDAX detector) in the STEM mode. For this particular investigation, the cross sectional specimens were prepared[2] by the sandwich method including ion beam milling. This method is illustrated in Figure 3.14 and described as follows:

1. cutting a barrier die into half,
2. gluing of both barrier surfaces onto each other,
3. sawing into a ~0.5-mm-thick specimen,
4. mechanical thinning down to a ~0.08-mm-thick specimen,
5. dimpling the cross-section down to <0.02 mm of a thickness, and
6. thinning the barrier cross-section using an ion beam milling (Precision Ion Polishing System Gaten PIPS 691).

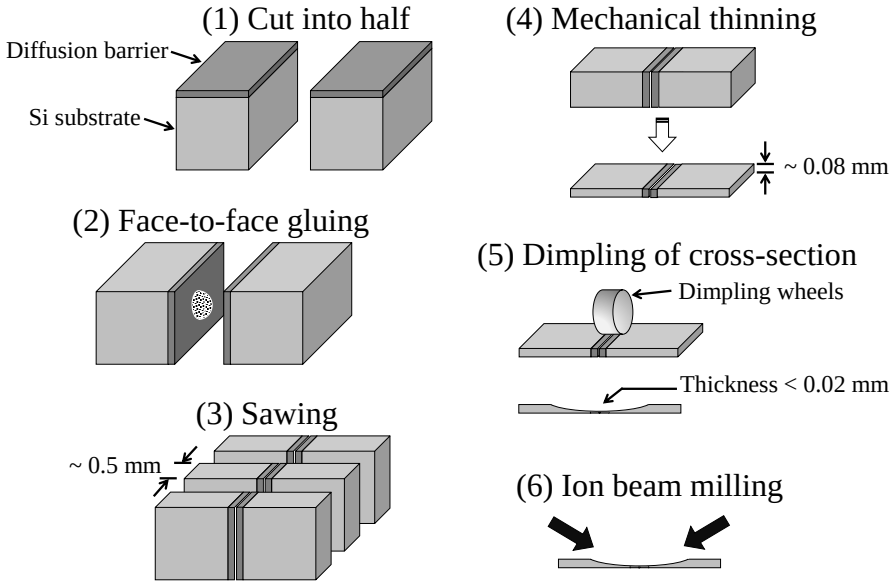

Figure 3.14: TEM specimen preparation.

TEM-EDX analysis

As electrons with high kinetic energy are accelerated through a thin specimen, several interactions, which are shown in Figure 3.15, between the accelerated electrons and the specimen's atoms will be produced. An EDX analysis utilizes characteristic X-rays for distinguishing between elements and for determining element's distribution from a very small region of a TEM specimen. The X-ray spectra show several characteristic peaks for each element contained in the region. These peaks are originated from an X-ray photon, which is generated when electrons are transferred from the outer to the inner atomic shells within an atom. This electron transfer is occurred due to electron vacancies produced as the accelerated electrons eject electrons in a low energy band or in the inner atomic shells. Consequently, these characteristic peaks can be

[1] Dr. Ulrich Schürmann
[2] Christin Szillus

related to the binding energy of an electron within an atom or an element [114]. Table 3.4 lists the electron binding energies of the contributed elements in the presented study.

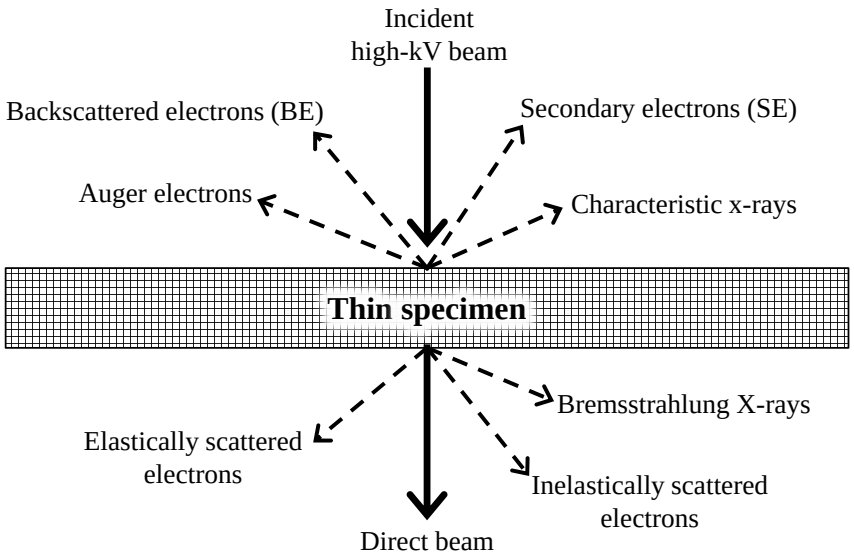

Figure 3.15: Interactions between an accelerated electron and a thin specimen.

Basically, an EDX analysis is performed using a very small beam of the accelerated electrons, typically <5 nm and at best <0.1 nm in diameter (in this study, it was 1–2 nm), which scan every point within an area so that the elements distribution can be mapped by combining the EDX analyses in the region of interest. This scanning principle in the TEM, namely Scanning TEM (STEM), can be employed to produce a bright field as well as a dark field STEM images. The bright field STEM image is produced by selecting only the direct beam, which is coming from the specimen, to hits a bright field detector. The dark field STEM image is produced by collecting only the scattered electrons, which are coming from the specimen, using an annular detector, namely Annular Dark Field detector. The incident electrons may be scattered at relatively high angles (>3°) after coming through the specimen, which contains of elements having usually a high atomic number. Therefore, a so-called High Angle Annular Dark Field detector is suitable to capture these electrons so that the resolution of the dark field STEM image as well as the EDX analysis can be enhanced [115]. An EDX line measurement in the STEM mode

Table 3.4: Electron binding energy of the contributed elements

Elements	Electron binding energy [keV]								
	K	L_1	L_2	L_3	M_1	M_2	M_3	M_4	M_5
7 N	0.4099	0.0373							
14 Si	1.839	0.1497	0.09982	0.09942					
22 Ti	4.966	0.5609	0.4602	0.4538	0.0587	0.0326	0.0326		
28 Ni	8.333	1.0086	0.87	0.8527	0.1108	0.068	0.0662		
32 Ge	11.103	1.4146	1.2481	1.217	0.1801	0.1249	0.1208	0.0298	0.0292
50 Sn	29.2	4.465	4.156	3.929	0.8847	0.7565	0.7146	0.4932	0.4849
73 Ta	67.416	11.682	11.136	9.881	2.708	2.469	2.194	1.793	1.735
74 W	69.525	12.1	11.544	10.207	2.82	2.575	2.281	1.872	1.809
79 Au	80.725	14.353	13.734	11.919	3.425	3.148	2.743	2.291	2.206

can also be performed across interfaces or grain boundaries in order to determine such diffusion phenomena. Furthermore, an EDX point measurement in the STEM mode can be performed for determining an atomic concentration within the interested region.

From Table 3.4, one can see that Si has only one significant electron binding energy (Si-K = 1.839 keV, which is close to the electron binding energies of W (W-M_4 = 1.872 keV) and Ta (Ta-M_4 = 1.793 keV). Therefore, the recorded Si-K profile could be similar to the recorded W-M and Ta-M profiles of the TiW-based and Ta-based barriers, respectively, in all line scan range as seen Figure 3.16-*left* and 3.16-*middle*. In order to determine and to plot the Si profile of the TiW-based barrier, the Si-K profile was subtracted with the W-M profile starting from a point, where their intensity is increased significantly and it is located at the interface between the Si substrate and the adjoining layer, to the end (top layer of barrier) of the EDX line measurement length as shown sequentially in Figure 3.16 from the left to the right. The same was applied for the Ta-based barrier in re-plotting the Si profile. In order to ensure whether only the "real" Si-K profile is obtained, the W-L and Ta-L profiles were also considered.

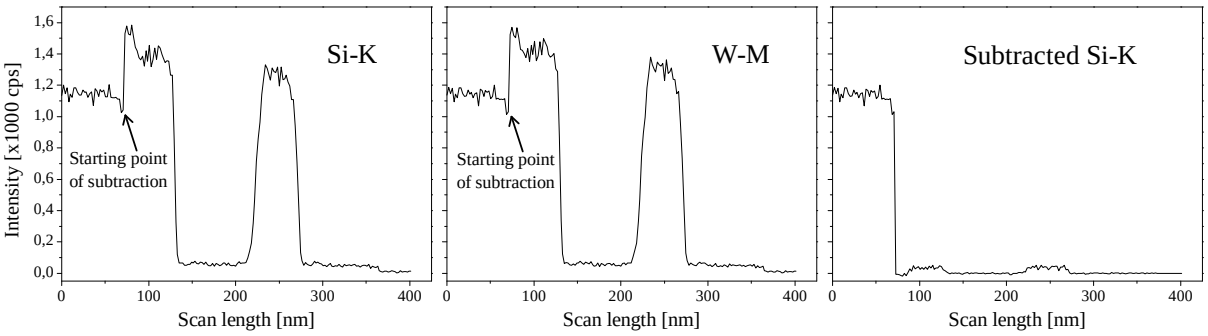

Figure 3.16: Procedure for obtaining an Si EDX profile for the non-annealed TiW-based barrier. For the rest of the EDX line measurements, the subtraction procedure can be seen in chapter A.1

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Energy Filtered TEM analysis

In EFTEM analysis, the direct beam imaging mode (bright field TEM image) is coupled with an EELS (Electron Energy Loss Spectrometry) principle to produce a filtered image or an elemental map. Different from the STEM-based mapping, which is a point-by-point scanning, the EFTEM image is recorded in parallel so that an energy-filtered image or an elemental map can be obtained in several seconds up to few minutes. The EELS principle is based on the amount of energy, which is lost after electrons undergo various inelastic scattering processes within a specimen. The electrons from the incident beam interact as well with the inner-shell (K, L, ...) electrons of atoms and thus lose their energy. These energy-loss electrons are shown as a step or an edge in the higher-energy-loss regime (>40 keV) of an EEL spectrum and are referred to as an ionization edge. An ionization edge determines an atomic structure of an element and is useful for an elemental analysis. Light elements, such as nitrogen, has a weak electron binding energy in the K shell that the high energy electrons from the incident beam will be scattered inelastically because it needs only small energy to eject electrons from K shell. The EELS utilizes those inelastically scattered electrons for determining an element. Normally, an EEL spectrometer is mounted at the bottom of the TEM column, so that a significantly high percentage of elastically and inelastically scattered electrons carrying elemental information from the area of interest can be collected through spectrometer. An energy filter in an EEL spectrometer usually

utilizes a magnetic prism, where scattered electrons are collected and deviated by 90° at least once to disperse on the basis of the energy of the electrons [116]. In this study a so-called GIF filter is used for the EEL spectrometer.

As explained above, it is concluded that the EDX and EELS analysis are suitable for investigating a high temperature reliability, such as diffusion phenomena, of barriers. It was employed in some works for determining structural alteration of barriers [24, 26, 29, 35, 40, 50, 51, 59]. It was employed as well in a similar work, where the diffusion of Ytterbium into the substrate was analyzed [117], with the presented study. In this presented study, the TEM analysis was performed on

1. the non-annealed and 24-h-annealed TiW-based and Ta-based barriers at 600 °C deposited on the *c*-Si substrate,
2. the 24-h-annealed TiW-based and Ta-based barriers at 600 °C deposited on the poly-Si and poly-SiGe layers, respectively, and
3. the 24-h-annealed barriers with a Au top layer at 600 °C deposited on the poly-Si layer.

3.3.4 Four-probe sheet resistance measurement

The measurement setup consists of a 4-probe measurement device (Polytec GmbH), an electrical current source, and a voltmeter. The device has four equally spaced tungsten carbide tips, which are supported by springs on the other end to minimize sample damage during probing, with 45° inclined angle. The tips are part of an auto-mechanical stage, which moves up and down during measurement. A DC current with 1 mA is applied to the outer tips while the voltmeter measures the voltage between the two inner tips. The measurement was performed before and after annealing at 200 °C, 300 °C, 400 °C, 500 °C, 600 °C and 650 °C. In each annealing temperature, 5 dies from each the TiW-based and Ta-based barriers were measured. The estimated accuracy of the resistance measurement is ±0.001 Ω.

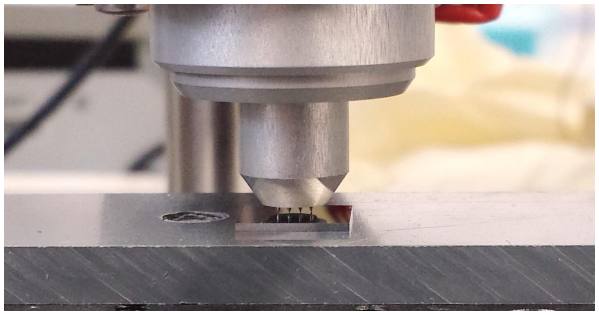


Figure 3.17: Four equally spaced tips touching down on a barrier die.

3.3.5 Adhesive tape test

The adhesion tape test is a simple method to evaluate the adhesion of sufficiently thick top layers on a rigid or a flexible substrate. This test is based on DIN EN ISO 2409 standard that all barrier dies before the test were diced 15-µm-deep into the substrate to create lines in the X and Y directions with 1 mm of a distance between lines. After this line dicing, the dies were placed on a self-adhesion tape to hold them at the bottom of die and then an adhesion tape (TESA®transparent adhesive tape 15 mm of a width) was applied on the top of the die by pressing. By pulling the tape in one direction with an angle of ~60° (between pulled tape and the sample), the barrier could be delaminated from the substrate due to a low adhesion. The qualification of the delamination was determined through a classification showed in Figure 3.18, which gave four associated grades of the barrier adhesion. This test was performed on the TiW-based and Ta-based barriers before and after annealing at 600 °C.

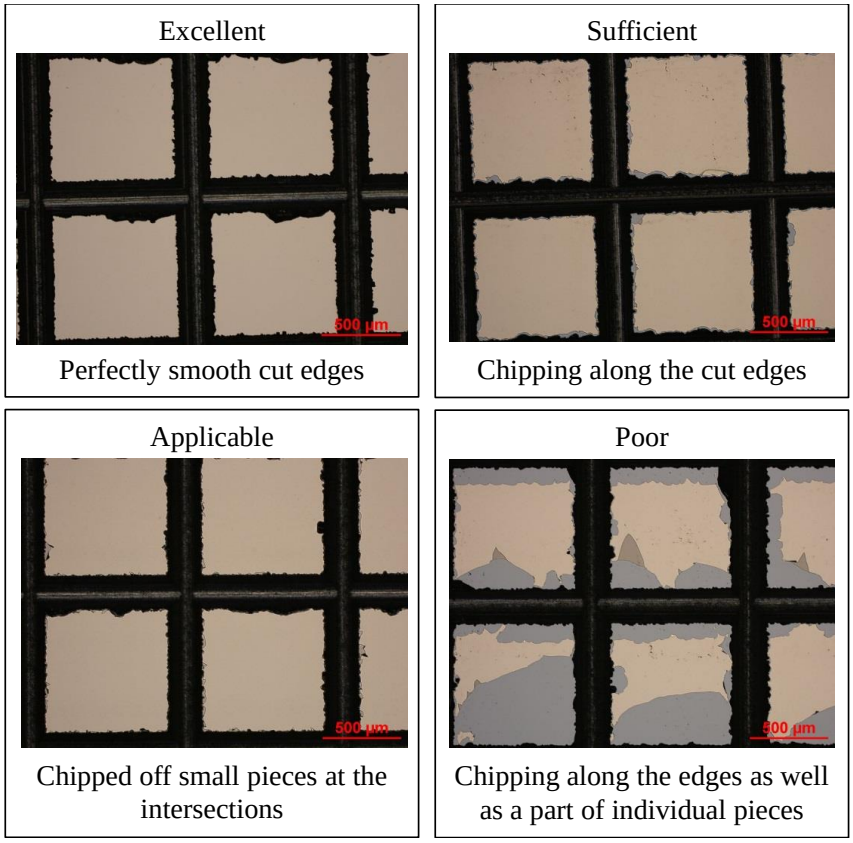


Figure 3.18: Classification of the adhesive tape test result.

3.3.6 Measurement using a transfer length method

The TLM measurement on the TLM structures having TLM Au pads was performed[3] at FhG-ISiT using an automatic measurement tool and based on the 4-probe measurement method. To provide this measurement, a special electronic circuit card was fabricated and a dedicated program was created. The circuit card has 16 probes in order to establish the electric contact on all 16 contact pads in a single TLM structure in one measuring time. The program managed an electric current input, a voltage reading, an electric resistance calculation and the automatic measurement so that all TLM structures on a wafer can be measured without time consuming. After a probes-pads contact was established, the 4-probe measurement was performed sequentially starting from the two TLM pads having narrow TLM gap to two TLM pads having a distant TLM gap. In a TLM die, there were 60 TLM structures with 5 different TLM gap types (G10, G20, G40, G60, and G80) and 6 different TLM pads width Z (70 µm, 100 µm, 120 µm, 200 µm, 300 µm and 500 µm). The number (10, 20, 40, 60, and 80) of the TLM gap types corresponds to the smallest spacing in micrometer between the first and the second TLM pads (see Figure 3.5 for the detail). In a wafer, there were 26 TLM dies and each 13 dies of them were distinguished from the distance between TLM pad's edge and poly-Si layer's wall; 5 µm (TLM5) and 10 µm(TLM10). For a TLM structure, there were 7 measurements, therefore there were 10,920 resistance values from a wafer in total. The sheet resistance of the poly-Si layer as well as the contact resistivity from each TLM structure were determined by using the method described in chapter 2. Four 6"-wafers were used to fabricate the TLM structures. Two wafers

[3]Felix Heinrich

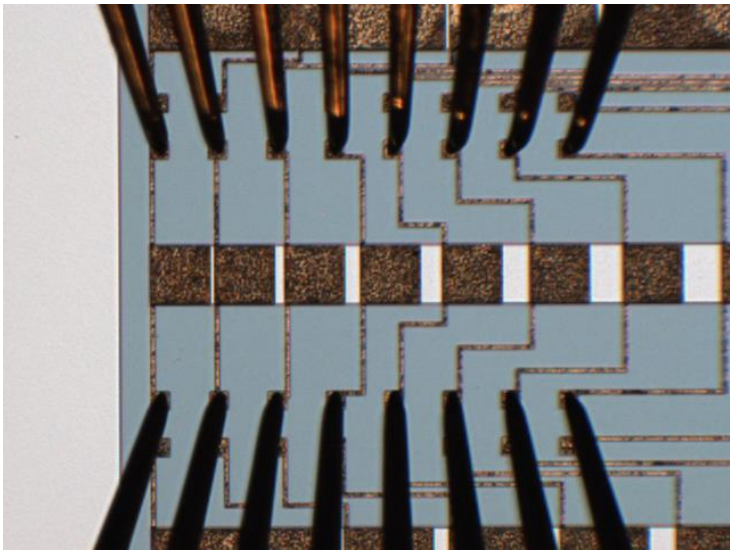


Figure 3.19: Contact establishment between 16 probes and 16 contact pads during an automatic TLM measurement.

had the TiW-based barrier with and without TLM Au pads. The other two wafers had the Ta-based barrier with and without TLM Au pads. After the fabrication, the TLM measurement on both wafers having the TLM Au pads was done at RT. After that, both wafers were annealed at 200 °C for 24 h in a vacuum chamber, which is adequate for an 8"-wafer as well. After cooling down the wafers, they were measured again and then were brought to annealing at 300 °C for 24 h. This sequence was performed up to 650 °C of annealing.

The TLM measurement on the TLM structures without the TLM Au pads was performed manually and based on the 4-probe measurement method as well. To provide the electric resistance measurement of a TLM structure, a setup with four manipulators and a multimeter (Keithley 2000) was prepared. Each manipulator has a metallic tip, which can be moved in micron range in x, y, and z directions, for establishing an electrical contact with a contact pad. The multimeter has a dedicated 4-point measurement feature to measure an electrical resistance. Figure 3.20 shows an example of some TLM dies and a TLM structure under measurement. An

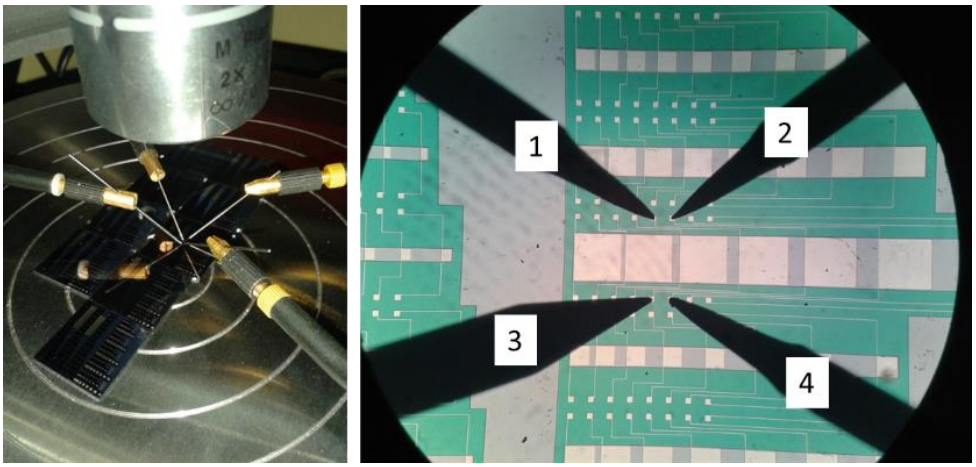


Figure 3.20: TLM dies under measurement using 4 manipulators (*left*), and a light microscope image showing a TLM structure under measurement (*right*).

electrical current has been applied from Tip 1 to Tip 4 while voltage difference was measured between Tip 2 and Tip 3. There were 7 measurements in each TLM structure due to 7 TLM gaps (see Figure 3.5 for the detail). The measurement was performed before and after annealing at 300 °C, 400 °C, 500 °C, 600 °C and 650 °C. Five TLM structures have been measured in each annealing temperature. They were

1. two structures of G80 having $Z = 500\,\mu m$ and $300\,\mu m$,
2. two structures of G60 having $Z = 500\,\mu m$ and $300\,\mu m$, and
3. one structure of G40 having $Z = 500\,\mu m$.

3.3.7 Scanning electron microscopy – EDX analysis

The SEM images were captured using an analytical tool (Carl Zeiss ULTRA Plus) with a varied EHT, an InLens and an SE2 detector, 30 µm of an aperture size, and 7–10 mm of working distance. The tool is equipped with an EDX analytical tool (OXFORD Instrument), which was utilized to determine the diffusion into the poly-Si and poly-SiGe layers and the composition of the Ni-Sn bond solder. The EDX analysis was performed with EHT = 26 kV, the SE2 detector, 60 µm of an aperture size, 10–15 mm of a working distance, and a dedicated software (OXFORD Instruments AZtecEnergy) to record the analysis. This high EHT was chosen because the electron with this energy can break the electron bond of Sn in K shell, which has $K\alpha_1$ ≈25.27 keV of an electron binding energy. Both EDX surface and point measurements were performed. For the EDX surface measurement, the cross-section of the poly-Si and poly-SiGe layers, which were annealed at 600 °C for 24 h, was analyzed. For the poly-Si layer, the TiW-based barrier with and without a Au top layer was deposited on the top before annealing. For the poly-SiGe layer, the Ta-based barrier with and without a Au top layer was deposited on the top before annealing. For the EDX point measurement, the cross-section of the non-annealed and 24-h-annealed Ni-Sn bond solder at 600 °C was analyzed.

An important phenomena in electron microscopy is the X-ray spatial resolution generated due to electron scattering events within the electron interaction volume, which can be occurred during EDX analysis. Generally, the interaction volume has a height of 1 µm below a specimen's surface and has a pear-shaped volume, which depends on the electron beam energy impinged on the specimen's surface, on the atomic number, and on the mass density of a specimen [19]. Therefore, if an EDX analysis is performed on a surface of a cross-section of a layer having <1 µm of thickness, then the generated X-ray can also be from the adjacent layer because the interaction volume crosses over the interface. If the shape of the interface is not flat, then the crossed-over interaction volume has a large part, thus more X-ray generated from other layer adjoined to the layer of interest as it can be seen in Table 4.6. Therefore, the element determination from a single element layer would be challenging because the element from the adjoined layer could also be determined.

To prepare the poly-Si and poly-SiGe cross-sections, a barrier die was cut into half. The surface on the broken side (cross-section) was taken for the EDX surface measurement. The Ni-Sn bond solder cross-section was prepared by polishing a bonded die, which had been covered with an epoxy, until the bond solder structures were exposed. After that, the cross-section was deposited with silver with ∼10 nm of a thickness.

3.3.8 Electrical characterization of the TLP bond solder

The characterization was performed by measuring the electrical resistance of daisy chain dies from a bonded wafer manually. After the fabrication of Ni-Sn TLP bond solder, 64 daisy chain dies were measured and 24 dies from them were annealed at 600 °C for 24 h and then were measured again. The measurement setup was the same with the one in the TLM measurement of the TLM structures without the TLM Au pads. A schematic design of a daisy chain structure, a daisy chain die, and a sketch of a bond solder are shown in Figure 3.21. There are 62 bond solder structures in a daisy chain die. The estimated accuracy of the resistance measurement is ±0.01 Ω.

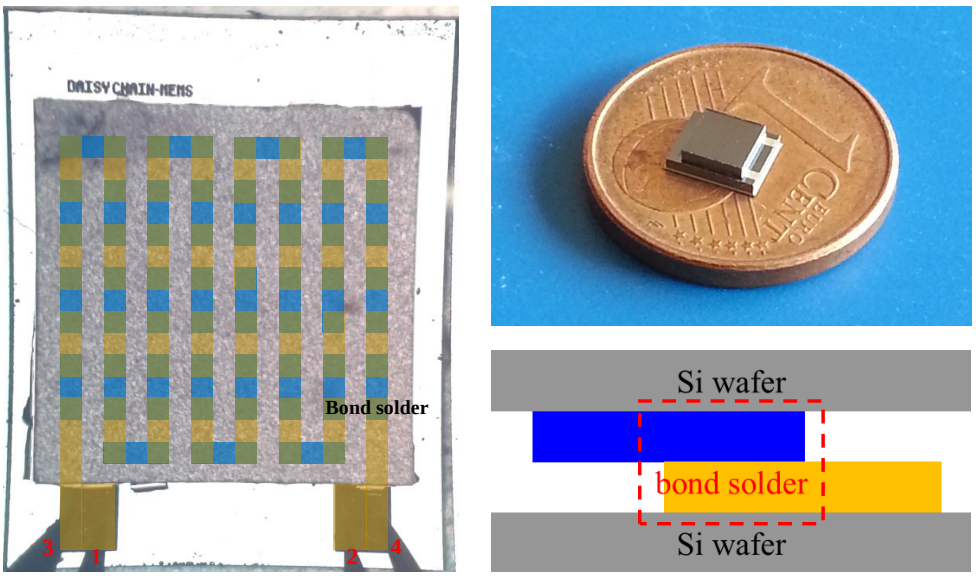


Figure 3.21: A daisy chain die (bottom-right), a schematic design of a daisy chain structure (*left*), a cross-sectional sketch of a solder contact (*bottom-right*), which is from the indicated inset.

3.3.9 Mechanical characterization of the TLP bond solder

The characterization consists of two investigations, which are a shear test for determining the bond strength of the bonded dies and a breaks analysis for determining the bond solder qualitatively. To perform the investigations, dies with a 16×16-array of a $100 \times 100\,\mu m^2$ bond structure distributed over a bonded wafer were taken. The number of dies, which were investigated, was 18 and 20 dies for before and after annealing (at 600 °C for 24 h), respectively. Figure 3.22 shows a bonded die with the 16×16 array of the bond solder (schematically drawn) which is ready for the shear test.

The Shear test is performed using a dedicated tool (DAGE 2400PC and Series 4000 Bond tester) with 100 kg load of a shear tool. This test is also based on MIL-STD-883G (Method 2019.7) standard [118]. The shear tool moves toward the top substrate of a bonded die while the bottom substrate is held by a body stop. The movement will stop instantaneously as the top substrate detached from the bottom substrate. The movement's length and the applied load are recorded for evaluating the bond strength of a bond solder. The minimum bond strength, which a bonded die must withstand a load, is defined in the standard as well. For this work, the bonded die should have 12.4 MPa (2.5 kg) or 24.8 MPa (5 kg) of a minimum bond strength

(shear force).

The breaks analysis is performed by inspecting visually at which location the break occurs on a bond solder after the shear test. The quality of a bond solder will be defined by counting a distribution percentage of the break locations within a bond solder. A break will occur at the weakest location in a bonded die. Five locations on a bond solder were defined in this work. They are

1. Substrate: the break occurs within the Si substrate,
2. Oxide: the oxide layer is delaminated from the Si surface or broken,
3. Diffusion barrier: the barrier is delaminated or broken,
4. Bond solder: the bond solder solder is delaminated from the barrier, and
5. Within bond solder: the break occurs within the layers of a bond solder.

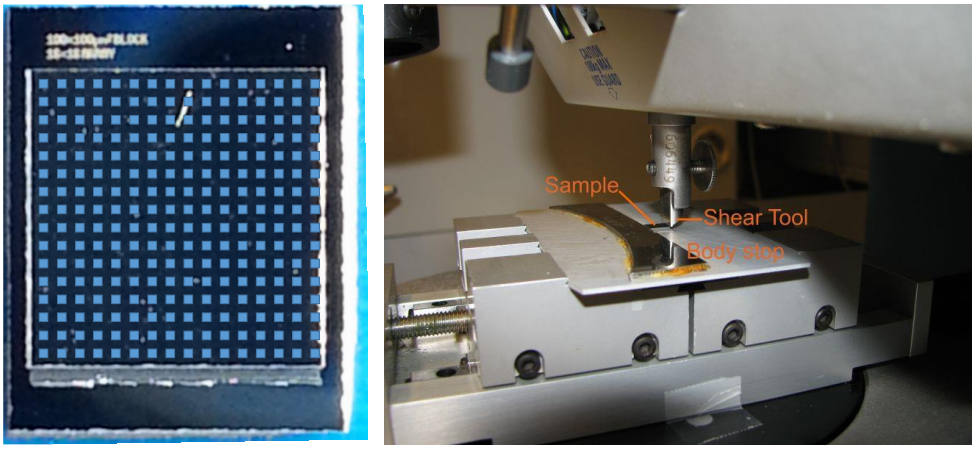


Figure 3.22: A bonded die with a 16×16 array (blue squares) of a bond solder (*left*), which is schematically drawn on the top wafer. Shear test die (sample) holder (*right*).

Chapter 4

Results

4.1 Measured wafer stress after the barrier fabrication

The measured barrier stress, which caused wafer curvature after barrier fabrication, is shown in Table 4.1. After the deposition of a 100-nm-thick Ta layer for the Ta-based barrier, the measured stress was 712 MPa that the wafer was induced by a tensile stress. After the deposition of a 100-nm-thick TiN layer on the Ta layer, the measured stress became −579 MPa that the wafer was induced by a compressive stress. After the deposition of another 100-nm-thick Ta layer and then a 100-nm-thick Ni layer, the wafer was induced back by the 875-MPa tensile stress. This deposition procedure shows that the TiN layer can be deposited for compensating the induced tensile stress, so that the final wafer curvature can be reduced as low as possible.

Table 4.1: The measured barrier stress after the fabrication of the TiW-based and Ta-based barriers with the measured barrier stresses after deposition on an 8"-wafer. Positive or negative stress is related to the tensile or compressive stress, respectively.

TiW-based barrier			**Ta-based barrier**		
Deposition of	Thickness [nm]	Average wafer stress [MPa]	Deposition of	Thickness [nm]	Average wafer stress [MPa]
Ta	20	456	Ta	100	712
TiW	40	} -321	TiN	100	-579
TiN	100		Ta	100	474
TiW	40		Ni	100	875
Ni	100	133			
Ta/TiW/TiN/TiW/Ni, total thickness: 300 nm			Ta/TiN/Ta, total thickness: 400 nm		

The same also occurred for the TiW-based barrier that the TiN layer can serve as a stress compensation. After the deposition of 180-nm-thick stacked layers (TiW/TiN/TiW), the measured stress was −321 MPa. Therefore, after the deposition of a 100-nm-thick Ni layer, the measured tensile stress and thus wafer curvature can be maintained as low as possible. Because sandwiching of the TiN layer with the TiW layer was performed in a time inside a sputter chamber, the stress in-between layers was not measured.

4.2 Reliability investigation of the TiW-based and Ta-based barriers

4.2.1 XRD analysis

Barriers deposited on the *c*-Si substrate

The X-ray diffractograms in Figure 4.1 show peaks of phases contained in both barriers before and after annealing. The peaks of the expected phases of each barrier are based on the Joint Committee on Powder Diffraction Standards of the International Center for Diffraction Data (JCPDS-ICDD) [119] and indicated by the symbols at the bottom and at the top of the diffractograms for before and after annealing, respectively.

For the TiW-based barrier before annealing (RT), the peak at $2\theta = 40.3°$ belongs to a TiW phase (JCPDS-ICDD 491440), at $2\theta = 44.8°$ belongs to a Ni phase (JCPDS-ICDD 031051), and at $2\theta = 37°$ and $2\theta = 62.2°$ belongs to TiN phases (JCPDS-ICDD 870633). Peaks of Ta phases are not appeared because the Ta layer is the bottom layer in the barrier, where the upper layers could be the obstacles for the diffracted X-ray beam to reach the X-ray detector. Additionally, the Ta layer has a thickness of 20 nm, which is relatively thin to diffract a weak X-ray beam. The TiN peaks are shifted from $2\theta = 36.7°$ and $2\theta = 61.9°$ to $2\theta = 37°$ and $2\theta = 62.2°$, respectively, indicating that the TiN layer is under tensile stress.

For the Ta-based barrier before annealing (RT), the peaks at $2\theta = 44.8°$ and $2\theta = 52.1°$ belong to the Ni phase (JCPDS-ICDD 031051), and at $2\theta = 36.8°$ and $2\theta = 62°$ belong to TiN phases (JCPDS-ICDD 870633), at $2\theta = 34.2°$ belongs to a β-Ta phase, and the other three Ta peaks at $2\theta = 37.4°$, $2\theta = 38.2°$, and $2\theta = 39.4°$, which appear as a significantly broad β-Ta peak (JCPDS-ICDD 040788). The β-Ta peak is shifted from $2\theta = 33.7°$ to $2\theta = 34.2°$ indicating that the Ta layer is under tensile stress.

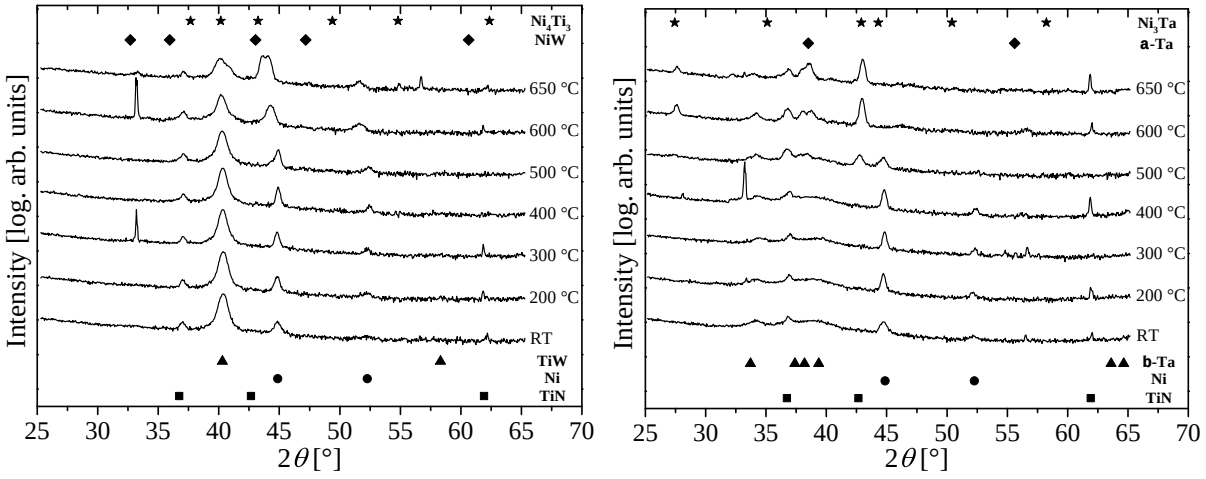


Figure 4.1: XRD diffractograms of the TiW-based (*left*) and Ta-based (*right*) barriers deposited on the *c*-Si substrate. The symbols are the peaks that belongs to the expected phases, which is written in the right side, from the barriers.

For both barriers, the Ni peaks at $2\theta = 44.8°$ and $2\theta = 52.3°$ are relatively broad due to a small grain size. Sharp peaks appeared at $2\theta = 33.2°$ in three plots stem from the *c*-Si substrate having the $\langle 2\ 0\ 0 \rangle$ crystal orientation.

After annealing, Ni peaks at $2\theta = 44.9°$ and $2\theta = 52.3°$ are sharpened starting from 200 °C to 400 °C of annealing for both barriers. This can be related to a recrystallization of the Ni layer producing large grains within the Ni layer. For the TiW-based barrier, there is an insignificant decrease of the TiW peak at $2\theta = 40.3°$ together with the broadening of the Ni peak at $2\theta = 44.9°$ (the left side of the peak's shoulder is less steep compared to this peak after 400 °C annealing) after 500 °C annealing. This can be related to an insignificant interdiffusion, which already took place between the Ni and TiW layers. After 600 °C annealing, both Ni peaks are disappeared together with the appearance of new peaks at $2\theta = 44.3°$ and $2\theta = 51.6°$ due to the growth of the Ni-TiW interdiffusing layer. The intensity of the TiW peak at $2\theta = 40.3°$ decreases due to this growth either. After 650 °C annealing, the TiW peak at $2\theta = 40.3°$ decreases and broadens (the right side of the peak's shoulder is less steep compared to the left side) that could stem from the Ni_4Ti_3 phase grown within the TiW layer, and the two adjacent peaks at $2\theta = 43.6°$ and $2\theta = 44.1°$ are appeared due to a possible phase growth when Ni, Ti, and W elements are mixed completely.

For the Ta-based barrier, the intensity of the Ni peak at $2\theta = 44.9°$ after 500 °C annealing decreases due to the interdiffusion between the Ni and the Ta layers indicated by the appearance of a new Ni_3Ta peak with a low intensity at $2\theta = 42.8°$. The disappearance of the Ni peak at $2\theta = 52.3°$ is due to the growth of the Ni_3Ta phase either. The β-Ta peak at $2\theta = 37.8°$ sharpens, so that the TiN peak at $2\theta = 36.7°$ becomes significant. After 600 °C annealing, all Ni peaks disappear and the Ni_3Ta peak sharpens together with the appearance of another Ni_3Ta peak at $2\theta = 27.4°$. This indicates that the Ni layer diffuses completely into the Ta layer. The α-Ta peak at $2\theta = 38.5°$ appears indicating a phase transformation temperature [50]. The shifting of the β-Ta peak from a high to a low diffraction angle at 500 °C, where it is relative to the its ideal position at $2\theta = 33.7°$, indicates that the tensile stress of the Ta layer is relaxed. This relaxation is followed with the increase of the α-Ta peak at $2\theta = 38.6°$ for higher annealing temperature that it may be caused by the incorporation of additional atoms into the α-Ta lattice [50]. After 650 °C annealing, the intensity of the α-Ta peak increases and both TiN peaks show an insignificant alteration as compared with those before annealing.

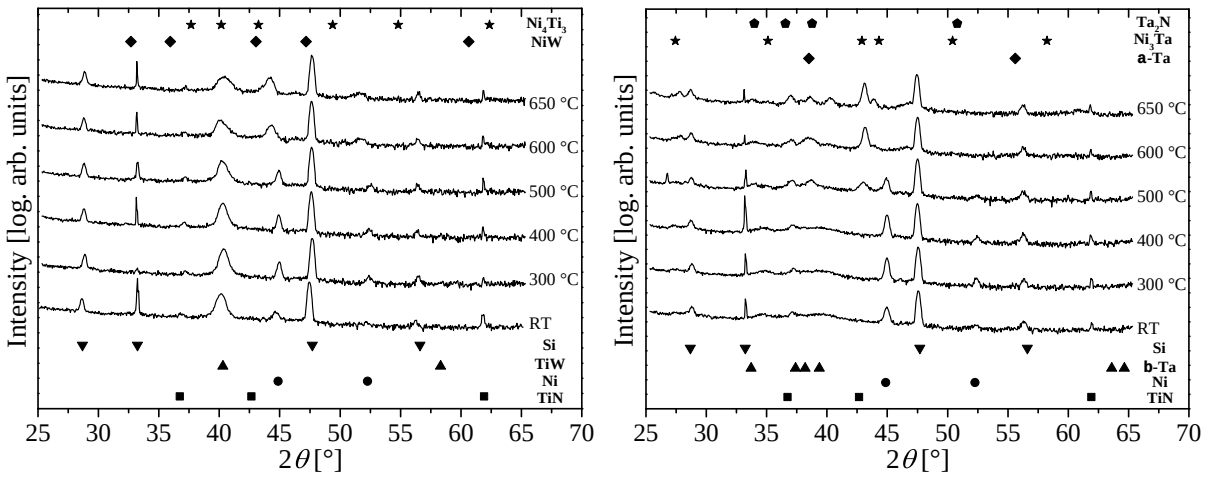


Figure 4.2: XRD diffractograms of the TiW-based (*left*) and Ta-based (*right*) barriers deposited on the poly-Si substrate. The symbols are the peaks that belongs to the expected phases, which is written in the right side, from the barriers.

Barriers deposited on the poly-Si layer

The impact of annealing has a similar result between the barriers deposited on the poly-Si layer and those deposited on the *c*-Si substrate as depicted in Figure 4.2. However, both Ni peaks for the Ta-based barrier decrease insignificantly after 500 °C annealing together with the appearance of a low Ni_3Ta peak at $2\theta = 43°$ (JCPDS-ICDD 180893). The the appearance of the Ni_3Ta peak, which is shifted from $2\theta = 27.4°$ to $2\theta = 26.9°$, could be due to a compressive stress induced within the barrier after 500 °C annealing. After 600 °C and 650 °C annealing, this peak is shifted to $2\theta = 27.8°$ due to an induced tensile stress within the barrier as a consequence of the growth of the Ni-Ta interdiffusing layer. It shows as well that, after annealing from 500 °C to 650 °C, the β-Ta peak is shifted back to its reference at $2\theta = 33.7°$ due to a layer stress relaxation. Three Si peaks from the poly-Si layer appear and have the highest peak at $2\theta = 47.7°$ indicating that the grains of the poly-Si layer have a preferred $\langle 2\ 2\ 0 \rangle$ orientation. Shifting of the Si peaks in the Ta-based barrier observed in the barrier dies at all annealing temperatures indicates that the poly-Si layer is induced by a high intrinsic stress due to the presence of the barrier [120, 121]. In all four plots above, no silicide peaks up to 600 °C were observed.

4.2.2 TEM Analysis

Bright field images

The TEM bright field images of the barrier cross-section after fabrication are depicted in Figure 4.3. One can clearly see in Figure 4.3(a) and (b), that thin films are stacked, starting from the substrate to the Ni top layer, which corresponds to the barrier deposition sequence in Table 4.1. The TiW and Ta layers show a very dark contrast due to the high mass of W and Ta elements [114]. The TiW and Ta layers, which are adjoined to the Ni layer for the TiW-based and Ta-based barriers, respectively, show a brighter contrast than those adjoined to the substrate, because the latter has a thicker cross-section than the former after TEM sample preparation. Figure 4.3(c) shows higher magnification of the TiN layer in Figure 4.3(b), where one can clearly see its columnar structure and high surface roughness.

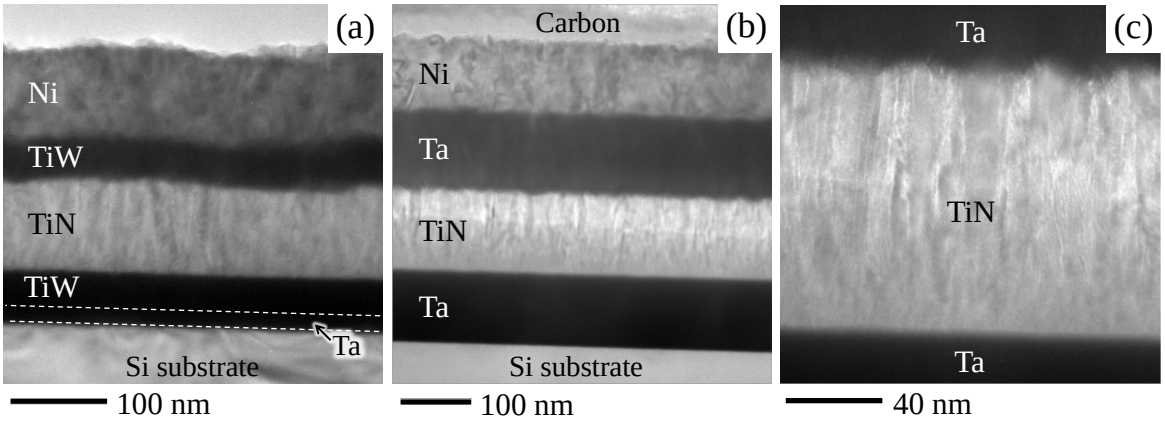


Figure 4.3: TEM bright field images of the non-annealed (a) TiW-based and (b) Ta-based barriers, and (c) the TiN layer. The carbon layer is a glue, which was used in TEM sample preparation.

After annealing, no alteration was observed either on the TiN layer or on the Ta/TiW and Ta layers, which are adjoined to the substrate, as observed in Figure 4.4. Significant alterations can

be observed on the Ni layer and on the adjoining TiW and Ta layers for the TiW-based and Ta-based barriers, respectively. The interface between the Ni layer and adjoining layers are more diffuse and rougher and the apparent thickness of these layers has decreased. These alterations could be related to the diffusion of Ni into the adjoining TiW layer as well as into adjoining Ta layer. In the Ta-based barrier, the grains within the interdiffusing Ni-Ta layer show a layered grain structure, which could be due to the difference of Ni-Ta phases. However, this interpretation can be proved by further investigation, for example using HRTEM. The TiW layer in the annealed TiW-based barrier has ~10 nm of grain size as depicted in Figure 4.4(c).

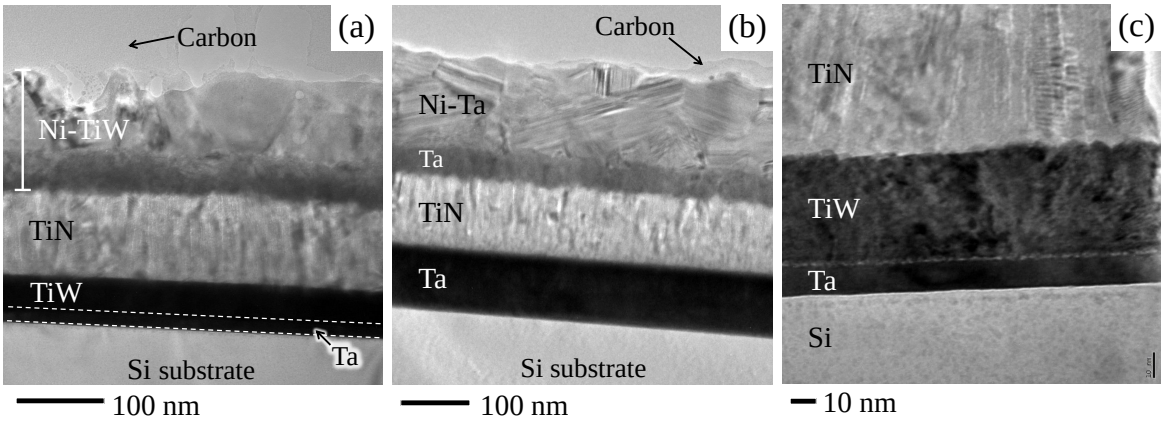


Figure 4.4: TEM bright field images of the annealed TiW-based (a) and Ta-based (b) barriers, and the magnification of the annealed TiW-based barrier showing a small grain size within the TiW layer (c).

The same occurrences were observed on the annealed TiW-based and Ta-based barriers, which were deposited on a poly-Si and poly-SiGe layers, respectively. In the bright field images of Figure 4.5, the interdiffusing Ni-TiW and Ni-Ta layers show a darker contrast rather than in Figure 4.4 due to the TEM specimen preparation, where the top part of barrier cross-sections was thicker than the bottom part. It should be mentioned that the interface between the barrier and the substrate remains sharp, which indicates no reaction occurred between the barriers and the Si substrate.

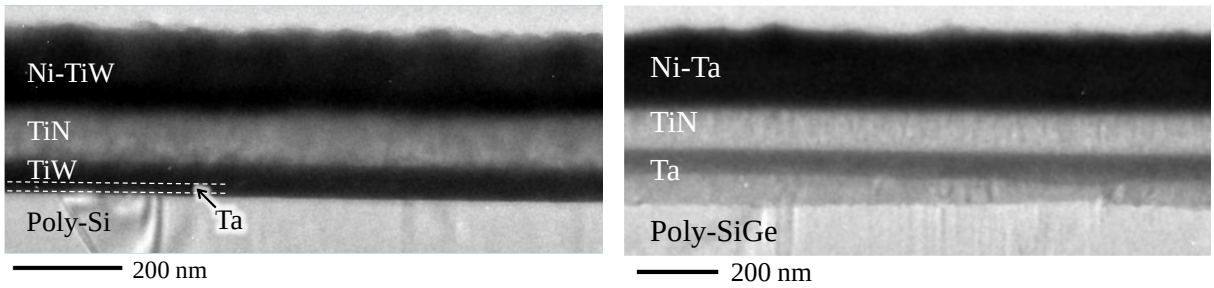


Figure 4.5: TEM bright field images of the annealed TiW-based (*left*) and Ta-based (*right*) barriers deposited on the poly-Si and poly-SiGe layers.

EDX elemental mapping

The element distribution within the barriers is provided by EDX elemental mapping as depicted in Figure 4.6. Before annealing, one can clearly see, that the elements are well-separated corresponding to the fabrication of stacked barrier layers. A faint Ti signal is observed in the

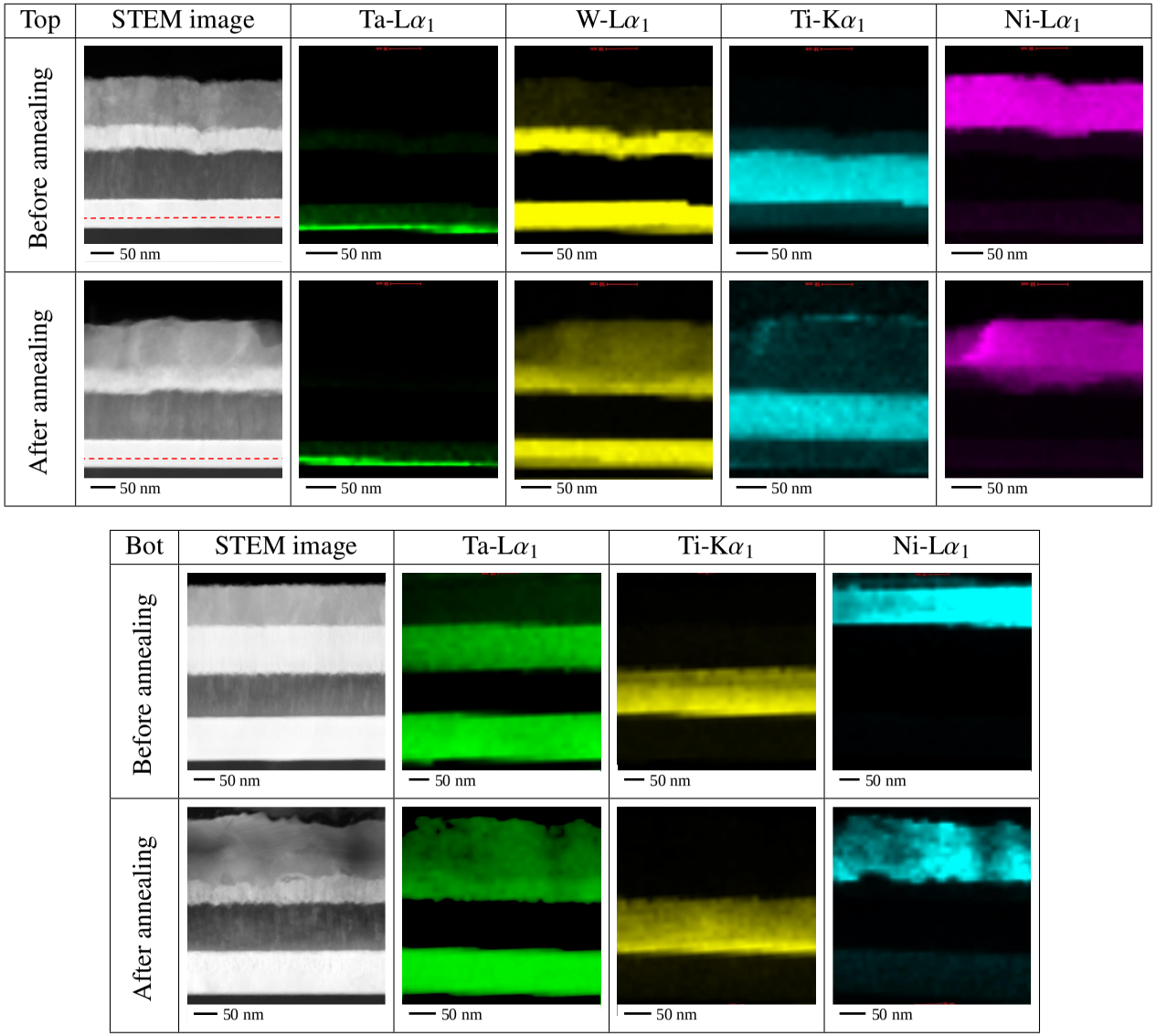


Figure 4.6: EDX elemental mapping of the TiW-based (*top*) and Ta-based (*bottom*) barriers deposited on a *c*-Si substrate.

sandwiching TiW layer due to the low amount of 10 at % of Ti. However, the mapping also shows a faint signal for elements, which are outside their corresponding layer, *i.e.*, a Ta signal in the sandwiching TiW layer for the TiW-based barrier, W and Ta signals in the Ni layer for the TiW-based and Ta-based barriers, respectively. The reason for the observed faint signal will be further investigated in Chapter 4.2.2. After annealing, a faint signal of W and Ti elements appears in the Ni layer, and an Ni signal appears partly in the adjoining TiW layer as depicted in Figure 4.6-*top*. A significant signal of Ta and Ni elements appears in the Ni layer and in the adjoining Ta layer, respectively, as depicted in Figure 4.6-*bottom*. These appearances of elements after annealing prove that interdiffusion took place between the Ni and the adjoining layer during annealing. This interdiffusion confirms the XRD analysis. A faint Ni signal is also observed in the Ta layer, which is adjoined to the substrate. This will also be investigated in Chapter 4.2.2.

EDX analysis before annealing

Quantitative chemical analyzes were performed on non-annealed and annealed barriers starting from the Si substrate to the Ni top layer. Figure 4.7 shows the EDX line measurement profiles

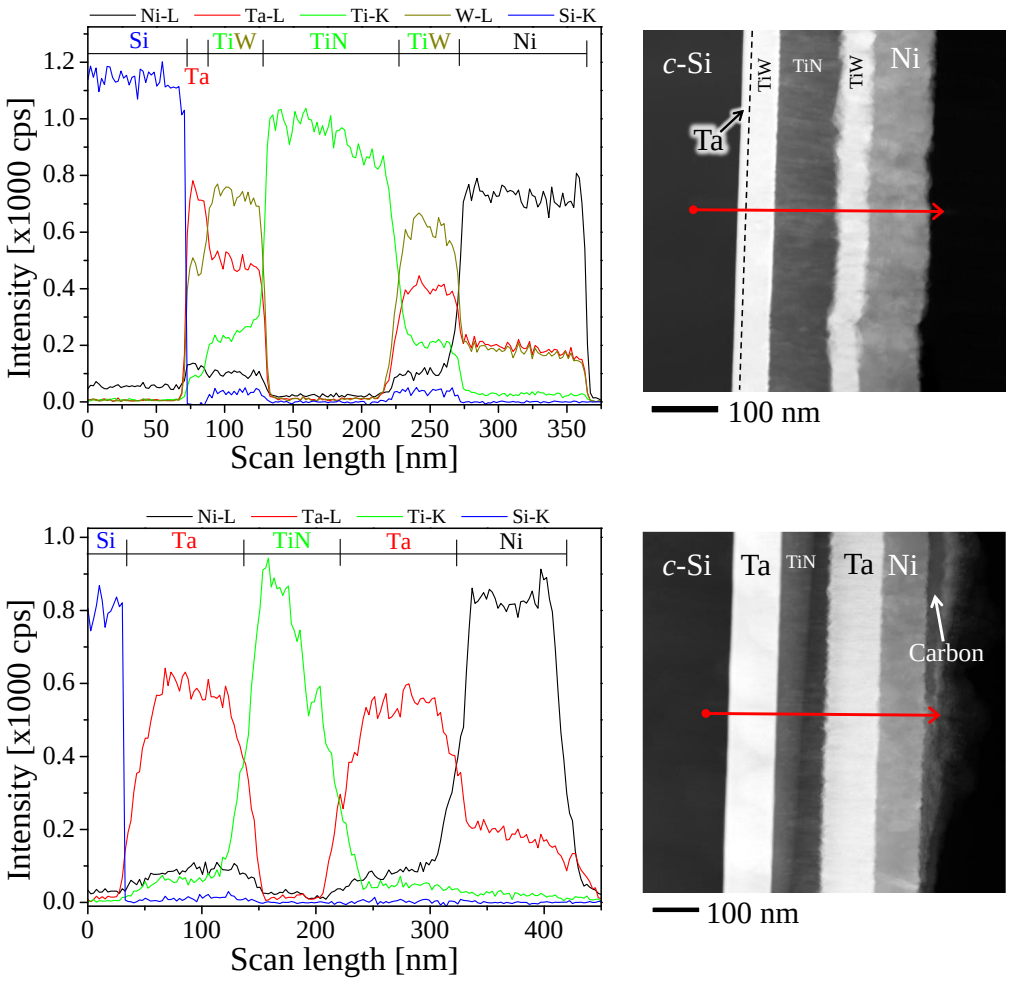


Figure 4.7: EDX line measurement profiles of the TiW-based (*top*) and Ta-based (*bottom*) barriers before annealing. On the right side, STEM images of the corresponding barriers, where the EDX line measurement (red arrows) was performed, are shown.

of non-annealed barriers, where the significant profiles are detected according to the stacked and well-separated layers. Here, one should expect no material diffusion. Consequently, a high intensity of an element's profile should be observed within its corresponding layer. However, similar to EDX elemental mapping in Figure 4.6, Ta and Ni profiles were observed in the sandwiching TiW layers as well as Ta and W profiles in the Ni layer for the TiW-based barrier. These additional profiles were also observed in the EDX profile of the Ta-based barrier, where a Ni profile was detected in the sandwiching Ta layers as well as a Ta profile in the Ni layer.

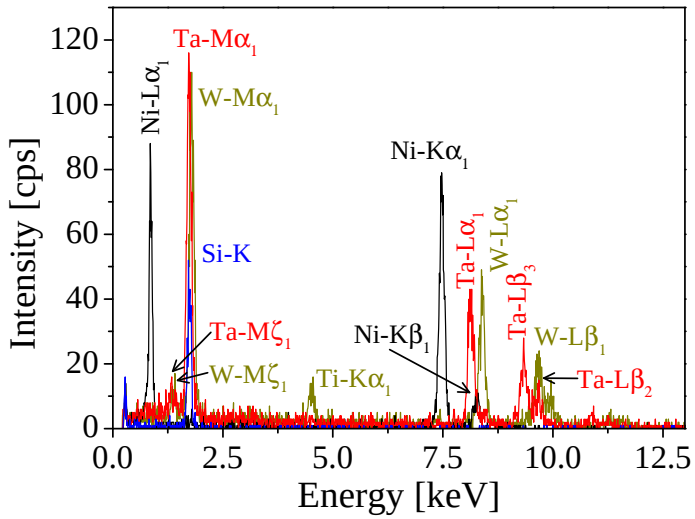


Figure 4.8: The comparison of the energy from Si, Ni and Ta elements, which observed in the TiW layer before annealing.

These additionally detected intensities, which also affect the EDX mappings, are due to multiple overlapping of the EDX-lines of the elements contained in the samples. Of course, this phenomenon hedges about the conclusion as to whether diffusion between the layers has taken place. To reveal these conditions, the spectrum of the TiW layer, which is close to the substrate from the non-annealed TiW-based barrier was taken and compared with the spectra of pure Ni, Ta, and Si as depicted in Figure 4.8. Because energies of Ta-Lα_1 and Ta-Lβ_2 were adjacent to those of W-Lα_1 and W-Lβ_1, respectively, the W-L profile interfered with the Ta-L profile, so that the Ta EDX profile has gained additional intensity from the W-L profile while the EDX detector was profiling the Ta element in the TiW layer. Background noise of energies of Ta-Mζ_1 and W-Mζ_1 interfered with the energy of Ni-Lα_1 as well, so that the Ni profile has gained low intensity in the TiW layer. The analysis of the Ni layer is the same as well, where Ta and W profiles have gained high intensity due to the adjacency of energies of Ni-Kβ_2 with Ta-Lα_1 and with W-Lα_1. For the spectra analysis on the layers having overlapping EDX profiles, the comparisons can be found in Chapter A.2.

Spectra of a Ta layer, which is adjoined to the substrate, were compared between the non-annealed and annealed Ta-based barriers in order to determine, whether the faint Ni signal observed in Figure 4.6-*bottom* was due to Ni diffusion after annealing. This comparison is depicted in Figure A.5(b), which shows similar spectra before and after annealing. Therefore, it is determined that the faint Ni signal was not due to the diffusion of the Ni element.

EDX analysis after annealing

The overlapping profiles, which are due to the adjacency between energies of each element, were also observed in the EDX line measurement after annealing as shown in Figure 4.9. These profiles are the Ta profile in the Ni and the sandwiching TiW layers for the TiW-based barrier, and Ni and Ti profiles in the Ta layers, which is adjoined to the substrate, for the Ta-based barrier. However, the Ni profile in the TiW-based barrier shows a significant intensity in the actual TiW layer, which is adjoined to the Ni layer, indicating a considerable Ni diffusion into the TiW layer. At the surface of the TiW-based barrier, a low intensity of Ti profile is observed. Spectrum analysis on this surface reveals that it contains of a high content of Ti as well as oxygen elements as depicted in Figure A.4. In the Ta-based barrier, the Ni profile shows a considerable intensity in a part of the Ta layer, which is adjacent to the Ni layer. This indicates that Ni diffuses into the Ta layer but not into the whole part of the adjoining Ta layer. The comparison to the bright field image (Figure 4.4-*right*) on the annealed Ta-based barrier indicates a Ni diffusion of ~70 nm deep into the Ta layer.

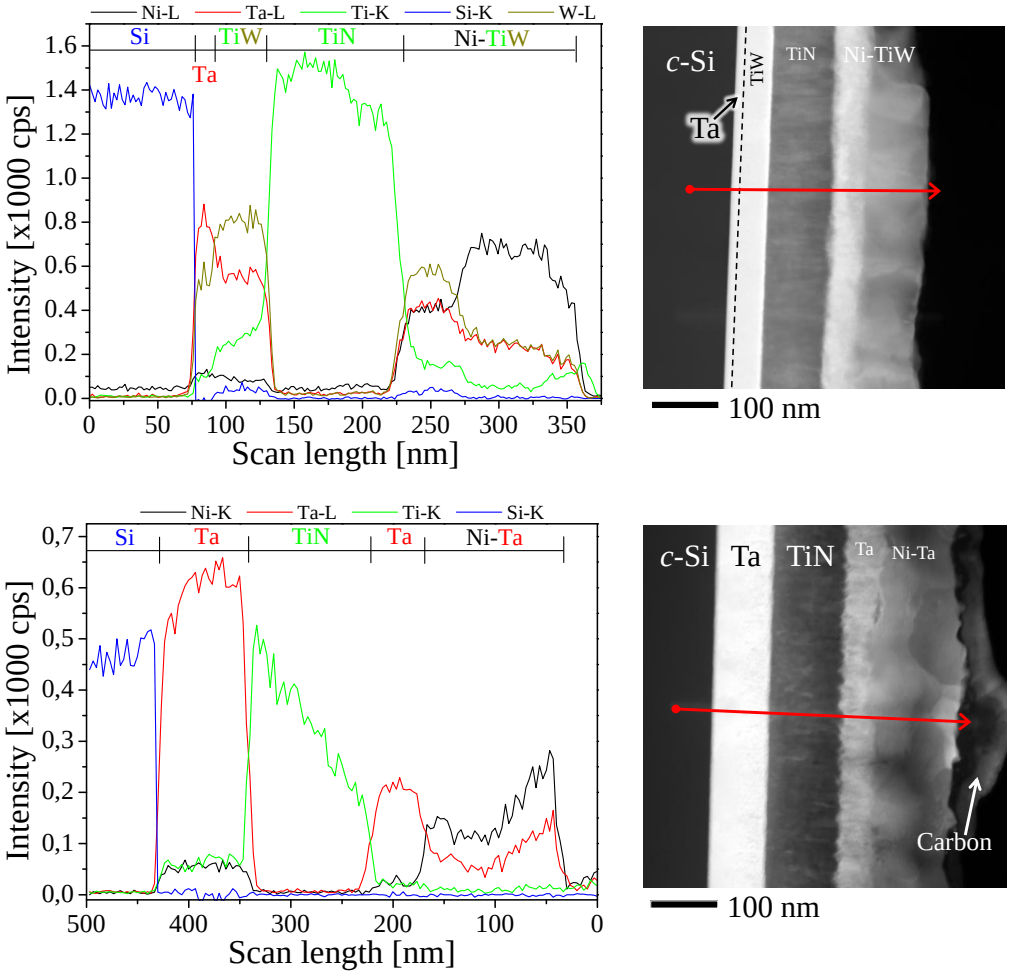


Figure 4.9: EDX line measurements of the TiW-based (*top*) and Ta-based (*bottom*) barriers after annealing. On the right side, STEM images of the corresponding barriers, where the EDX line measurement (red arrows) was performed, are shown.

Figure 4.10 shows the EDX line measurement, which was performed on the annealed TiW-based and Ta-based barriers deposited on the poly-Si and poly-SiGe layers, respectively. The

interdiffusion between the Ni and TiW layers as well as the Ni and Ta layers for the TiW-based and Ta-based barriers, respectively, is determined and observed clearly. In the Si substrate, all element profiles from both barriers show very low intensity, which indicates no diffusion into the substrate. Similar to the EDX analysis on the annealed TiW-based barrier deposited on *c*-Si substrate, the low intensity of a Ti element is observed as well at the surface of the TiW-based barrier. In the STEM images, a sharp interface is observed clearly between the poly-Si and the Ta/TiW layers as well as between the poly-SiGe and Ta layers in the TiW-based and Ta-based barriers, respectively. This sharp interface indicates no material diffusion into both Si layers.

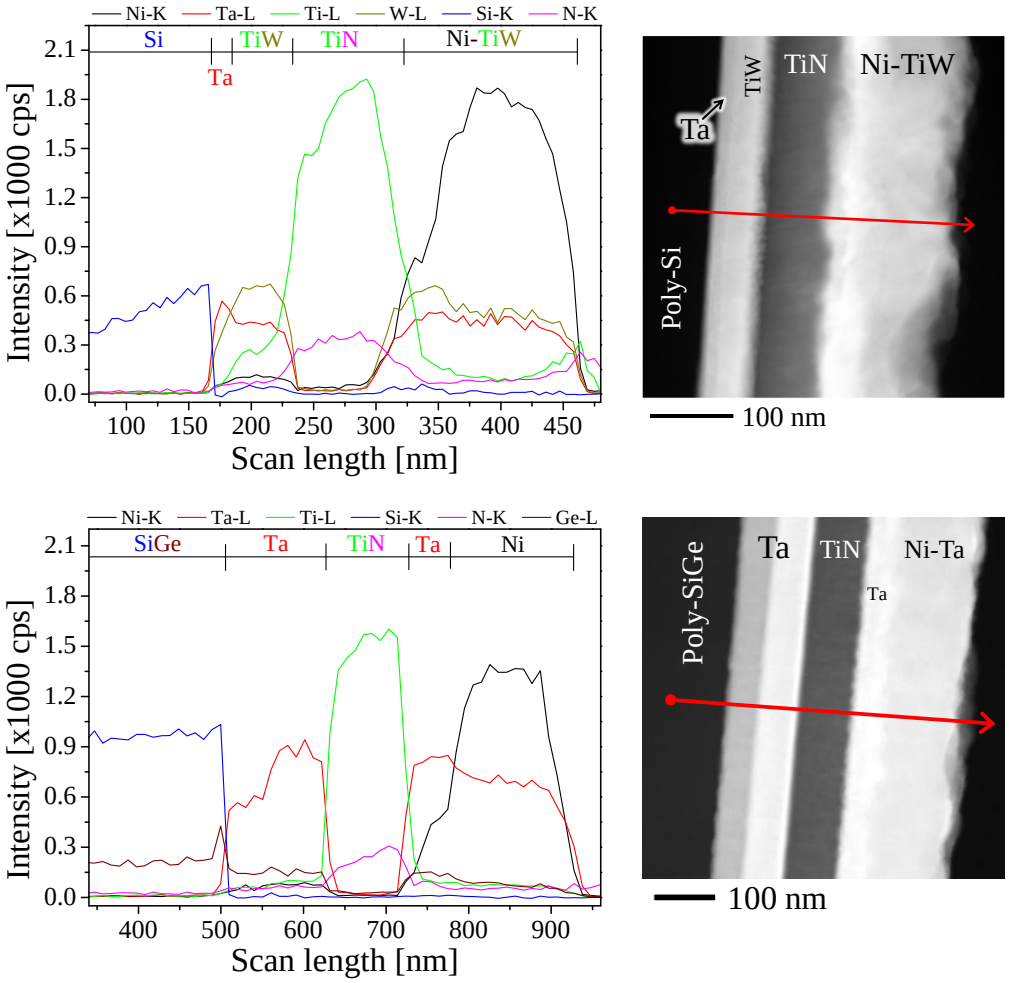


Figure 4.10: EDX line measurements of the TiW-based (*top*) and Ta-based (*bottom*) barriers deposited on the poly-Si and poly-SiGe layers, respectively, after annealing. On the right side, the STEM images of the corresponding barriers, where the EDX line measurement (red arrows) was performed, are shown.

A 100-nm-thick Au was sputtered on the top of the Ni layer in order to investigate the durability of both barriers towards Au diffusion after 600 °C annealing. Afterwards, an EDX line measurement was performed on both annealed barriers. In the TiW-based barrier, a Au profile was determined in all layers, except in a part of the Si layer as depicted in the EDX line measurement in Figure 4.11-*top*. An artifact with a sharp interface in the poly-Si layer (Figure 4.11-*top* on STEM image) was determined as a compound, which contained of Si, Au, and Ni elements. Additionally, Ti was determined on the top of the Au layer. In the Ta-based barrier, the Au was determined on the interface between the poly-SiGe layer and Ta layers as

depicted in the EDX line measurement in Figure 4.12-*bottom*. The measurement length of the Ta profile shown a longer profile than 100 nm. Different from the previous EDX analysis in Figure 4.9 and 4.10, there is a gap in the Ni profile between the Ni and adjoining Ta layers that can be indication of the delamination of the Ni layer. However, low Ni intensity, which could be originated from a thin Ni-Ta layer, was determined between the TiN and Ta layers.

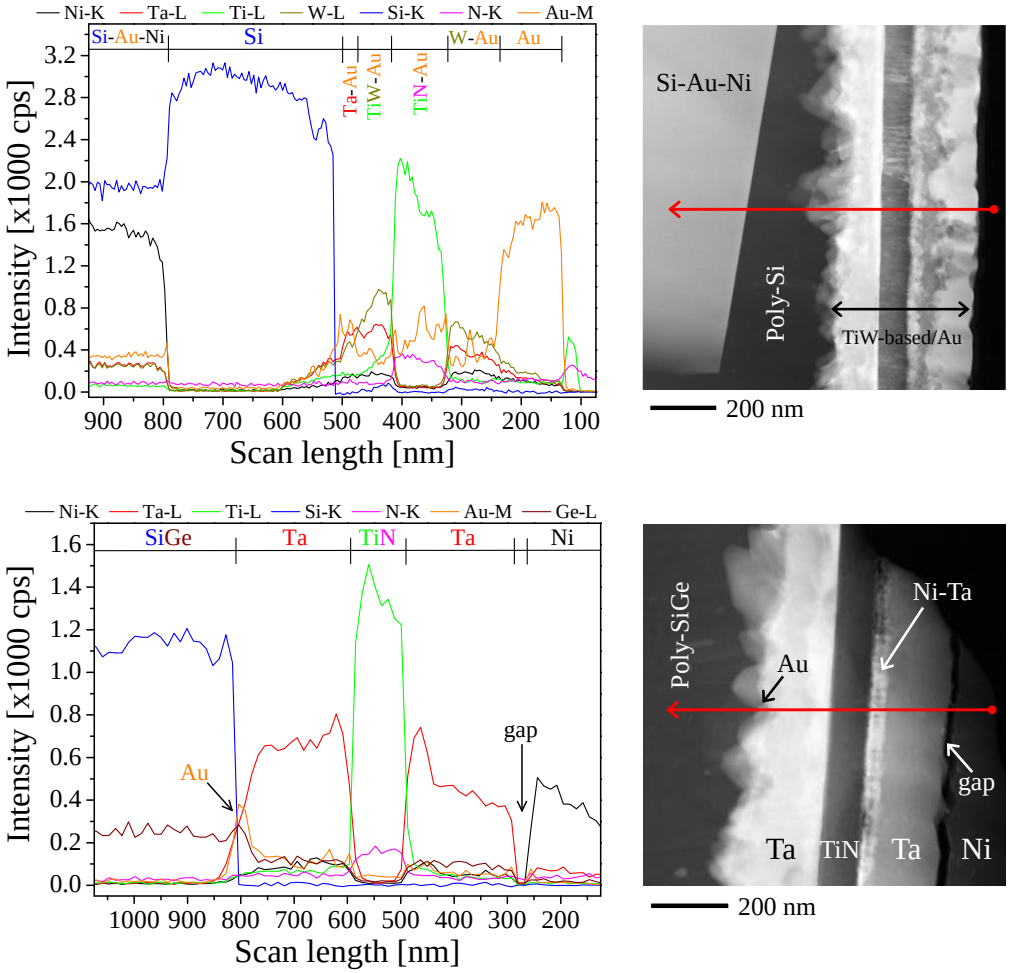


Figure 4.11: EDX line measurements of the TiW-based (*top*) and Ta-based (*bottom*) barriers with a Au top layer deposited on the poly-Si and poly-SiGe layers, respectively, after 600 °Cannealing. On the right side, STEM images of the corresponding barriers, where the EDX line measurement (red arrows) was performed, are shown.

EDX point measurement after annealing

To complete the quantitative analysis, several EDX point measurements were performed at the indicated locations on the cross-section of both annealed barriers as depicted in Figure 4.12. The results, shown in Table 4.2, reveal the composition of elements in interdiffusing layers (Point 1-4) and confirm that the overlapping profiles were not due to material diffusion (Point 5-7). The composition of the interdiffusing Ni-Ta layer (Point 3) shows approximately a ratio of 3:1 for the Ni:Ta ratio. Based on the Ni-Ta phase diagram, this ratio corresponds to a stable phase of Ni_3Ta compound [78]. It should be mentioned that the interface between barrier and substrate remains sharp, which indicates that no reaction occurred between the barrier and the

substrate.

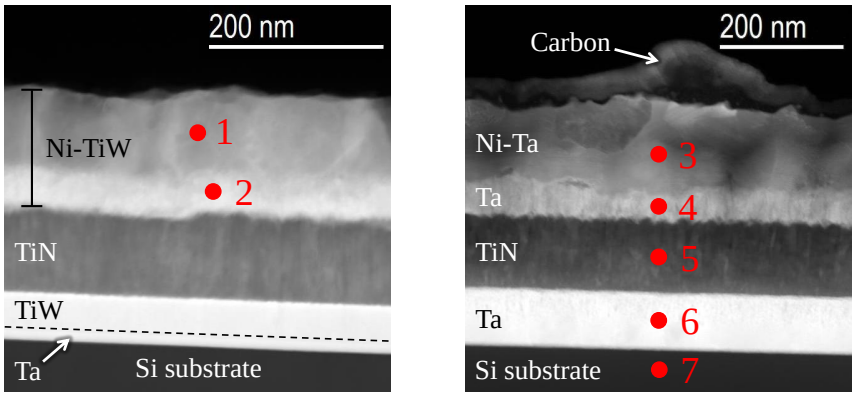


Figure 4.12: EDX point measurement on a specific location within each layer in the TiW-based (*left* and Ta-based *right* barriers after 600 °Cannealing.

Table 4.2: Element concentration, which was determined by the EDX point measurement on the indicated locations in Figure 4.12, for both annealed barriers.

Points	at.% of Ni	at.% of Ti	at.% of N	at.% of W	at.% of Ta	at.% of Si
1	91.9	2.8	-	5.3	-	-
2	57	12.1	30.9	-	-	
3	73	-	-	-	27	-
4	8.5	-	-	-	91.5	-
5	-	35.8*	64.2*	-	-	-
6	-	-	-	-	100	-
7	-	-	-	-	-	100

* The values were determined from the Ti and N profiles, which have energies adjacent to each other. However, at this point no other elements were determined except Ti and N.

EFTEM analysis on the Ta-based barrier

It had been reported that nitrogen diffused from tantalum nitride (TaN) layer to Ta neighboring layers as this type of stacked barrier (TaN layer sandwiched with Ta layers) was annealed at 600 °C [50]. In order to confirm, whether nitrogen could have been diffused as well from the TiN layer into the sandwiching Ta layers, Energy Filtered TEM (EFTEM) analysis was performed only on the non-annealed and annealed Ta-based barriers. Figure 4.13 shows the bright field images of cross-section from both Ta-based barriers and the corresponding EFTEM images. The EFTEM images from the annealed barrier is very similar to the one from the non-annealed barrier, thus obviously no nitrogen diffuses into sandwiching Ta layers.

With the exception of the Ni-Ta interdiffusing layer, Ta and Ti elements show a similar result before and after annealing either. The faint signal of Ni before annealing is intensified after annealing in the other stacked layers of the barrier. This is not an indication of Ni diffusion because an Ni element is not determined in the EDX analysis after annealing. An unexpected bright contrast at the interface between the Ta layer and the Si substrate could be due to Ta oxide, which grown due to reaction between Ta and native oxide on the Si surface. The bright contrast of each element after annealing shows a distinct interface between of them. This observation confirms the EDX analysis.

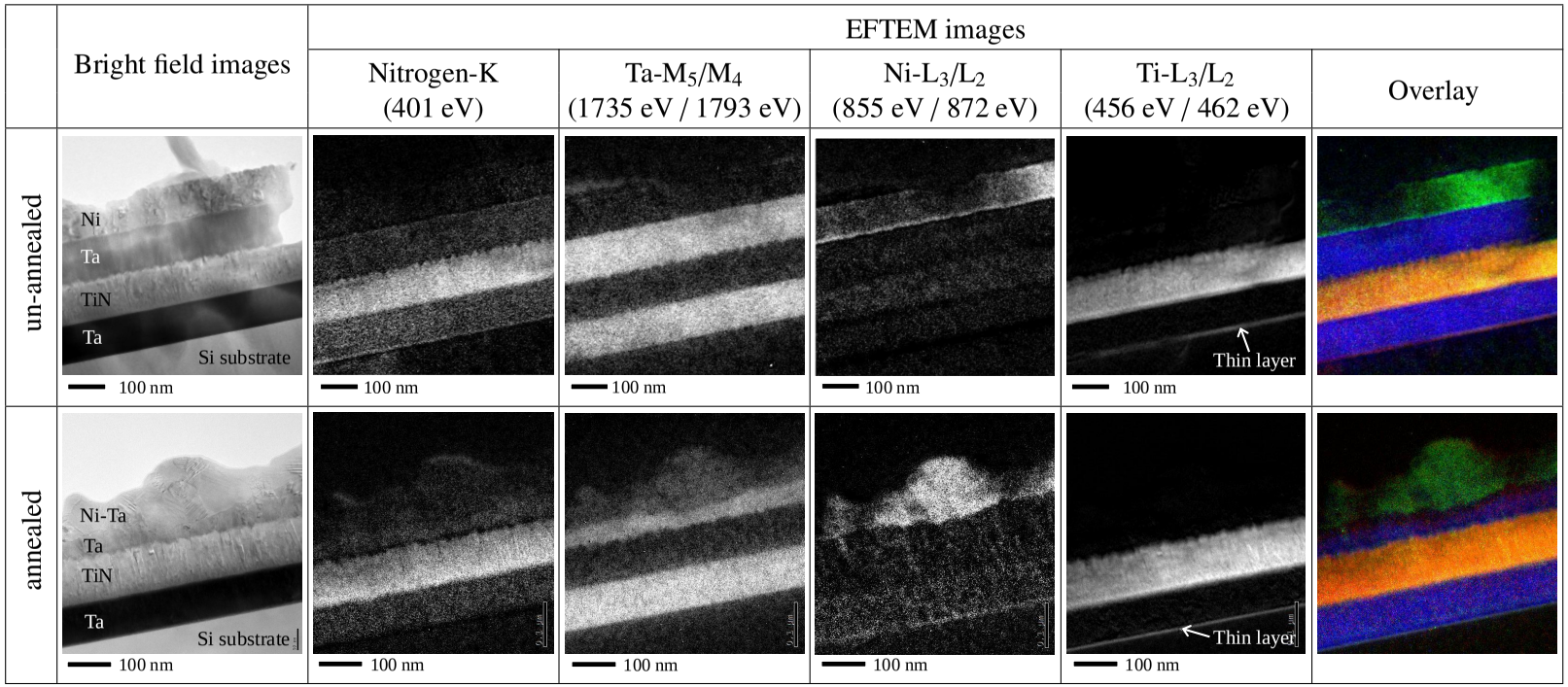


Figure 4.13: Cross-sectional EFTEM analysis of the non-annealed and annealed Ta-based barrier. The values below the element captions are the EEL edges, which were used in EFTEM analysis for determining the bright contrast in each element. Notes: Ni (*green*), Ta (*blue*), Ti (*yellow*), and N (*red*).

4.2.3 Diffusion investigation for the barriers on the poly-Si and poly-SiGe layers

Investigation for the barriers without a Au top layer

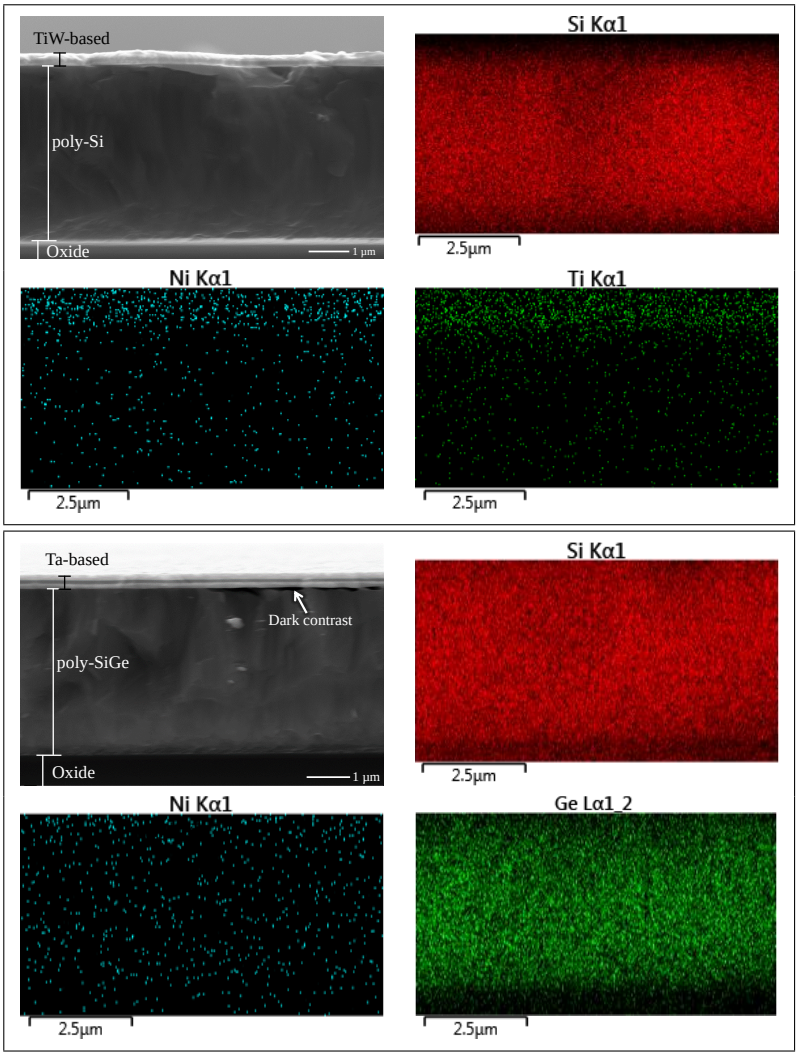


Figure 4.14: EDX surface measurement of annealed poly-Si and poly-SiGe layers with the TiW-based (*top*) and Ta-based (*bottom*) barriers, respectively. No materials were diffused from the barriers into poly-Si and poly-SiGe layers.

In order to determine material diffusion into the poly-Si and poly-SiGe layers, the EDX surface measurement was performed on both annealed barriers using SEM. The result is depicted in Figure 4.14 where a cross-section of the annealed poly-Si and poly-SiGe layers was analyzed. A signal of Ni and Ti elements was determined significantly on the upper side, where the barrier is located, of the poly-Si cross-section. A low Ni EDX signal was determined within the poly-SiGe cross-section due to background noise. A Si EDX signal was determined homogeneously within the poly-Si and poly-SiGe cross-sections. This investigation concludes obviously that materials were not diffuse from the barriers into both semiconductor layers after annealing. For the poly-SiGe layer, a Ge signal was also determined homogeneously within the cross-section. A dark contrast was observed on the interface between the Ta-based barrier and the poly-SiGe

layer. The oxide layer on the cross-sectional SEM image in Figure 4.14-*bottom* shows a dark contrast because the cross-section was tilted in such a way that the oxide layer was farther from electron gun than the stacked layers of the Ta-based barrier.

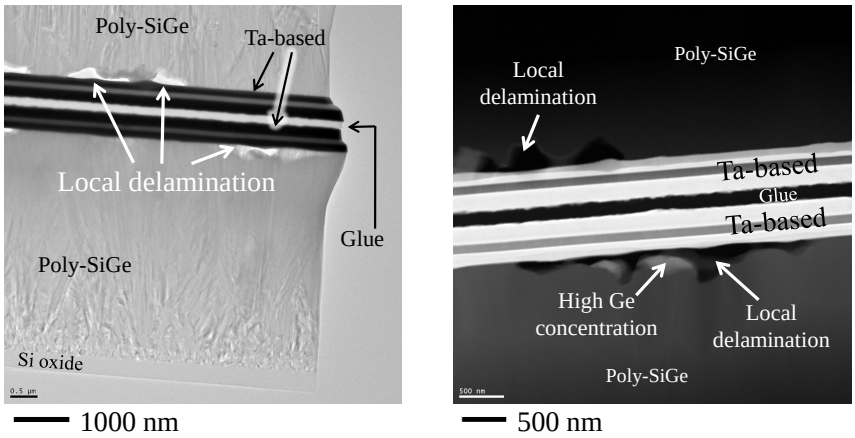


Figure 4.15: Bright field (*left*) and dark field (*middle* & *right*) TEM images of the annealed Ta-based barrier deposited on the poly-SiGe layer. A local delamination was observed between the poly-SiGe and the adjoining Ta layers. A layer with an irregular interface is observed between the poly-SiGe and the Si oxide layers.

The dark contrast, which is shown in the SEM image in Figure 4.14-*bottom*, is appeared to be a bright contrast in bright field image as shown in TEM images in Figure 4.15-*left*. This bright contrast is highly significant due to the edge effect and also because electrons are passing through the sample without hitting a layer. Therefore, this bright contrast in TEM image or the dark contrast in SEM image indicates a local delamination at the interface between the poly-SiGe and the adjoining Ta layers. The EDX point measurement on the bright contrast of the dark field image in Figure 4.15-*right* determined that the edge of poly-SiGe grains of the local delamination contains a high content of Ge atoms.

Investigation for the barriers with a Au top layer

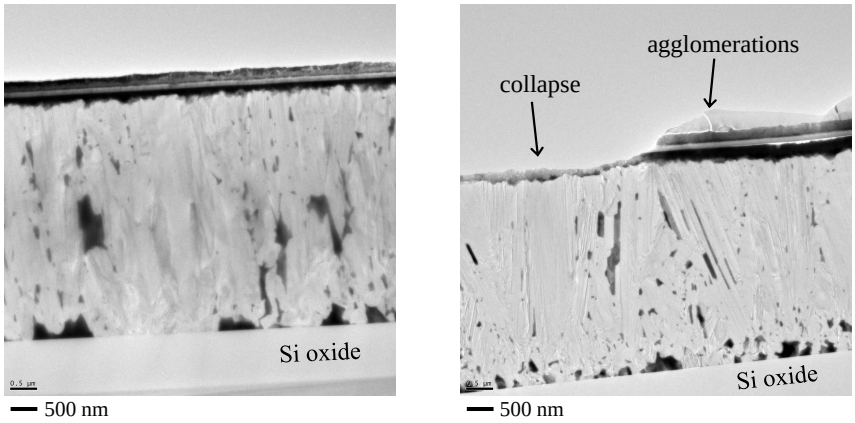


Figure 4.16: Bright field TEM images of the annealed poly-Si and poly-SiGe layers with the TiW-based (*left*) and Ta-based (*right*) barriers having Au over layer.

A 100-nm-thick Au deposited on the top of the barriers in order to investigate the durability of the barriers towards Au diffusion due to annealing. After annealing, a dark contrast is observed within poly-Si and poly-SiGe layers and it precipitates significantly at the interface between the poly-Si and the oxide layers, and between the poly-SiGe and the oxide layers depicted in Figure 4.16. The interface between the TiW-based barrier and the poly-Si, and between the Ta-based barrier and the poly-SiGe layers shows a coarse interface, which could be an indication of a material diffusion. On the top of the annealed Ta-based barrier, an agglomeration was grown and contained of a high concentration of Si atoms and a low concentration of Ni atoms after the EDX point measurement.

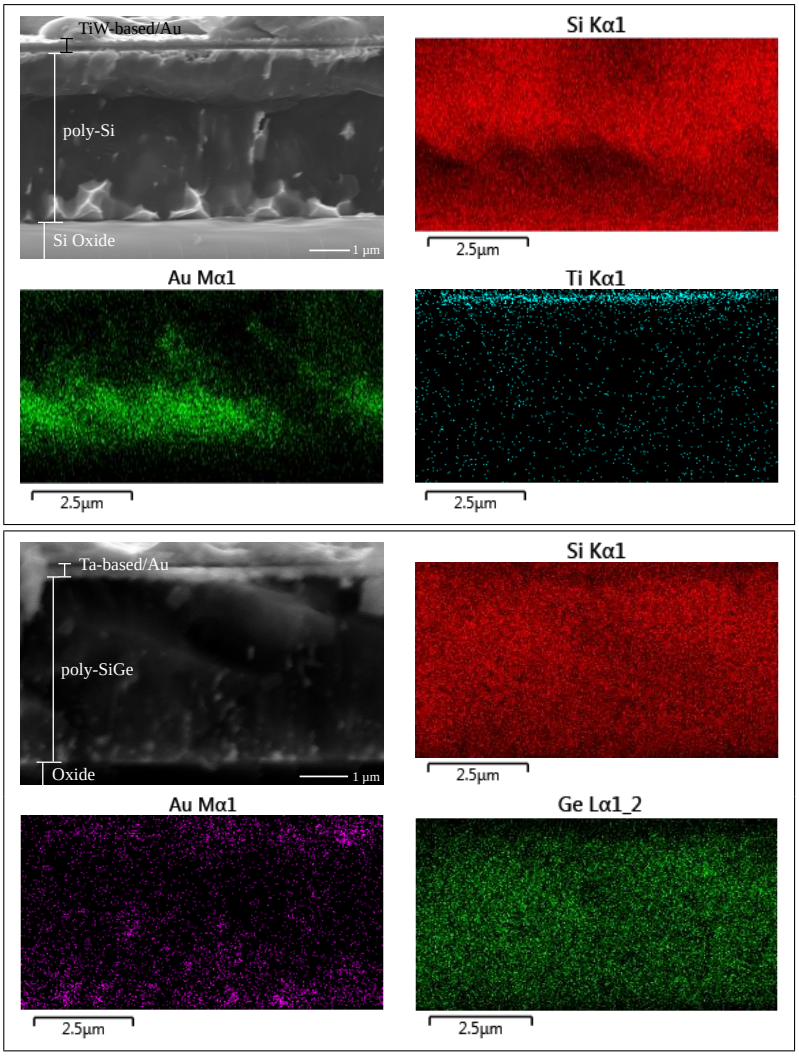


Figure 4.17: EDX surface measurement of the annealed poly-Si and poly-SiGe layers with the TiW-based (*top*) and Ta-based (*bottom*) barriers having Au over layer.

In order to determine the elements of the observed dark contrast in Figure 4.16, the EDX surface measurement was performed on both barriers using the SEM method. In Figure 4.17, a bright contrast is observed within the poly-Si and poly-SiGe layers and it precipitates on the Si oxide interface as well. This bright contrast, which is distributed within the poly-Si and poly-SiGe layers, is similar to the distribution of the dark contrast in Figure 4.16. The EDX analysis determined that this bright contrast belongs to Au, which has diffused from the top of

the barrier during annealing. The Ti EDX profile was determined significantly on the top of the poly-Si cross-section, where the TiW-based barrier was deposited. Figure A.6 in Appendix shows cross-sectional TEM images of artifacts resulting after the Au diffused into the poly-Si and poly-SiGe layers.

4.2.4 Sheet resistance (R_{sh}) measurement

Before annealing, the average of measured R_{sh} = 245 ± 0.82 mΩ and R_{sh} = 215 ± 1.06 mΩ for the TiW-based and Ta-based barriers, respectively. After annealing, both barriers exhibited R_{sh} increase as depicted in Figure 4.18.

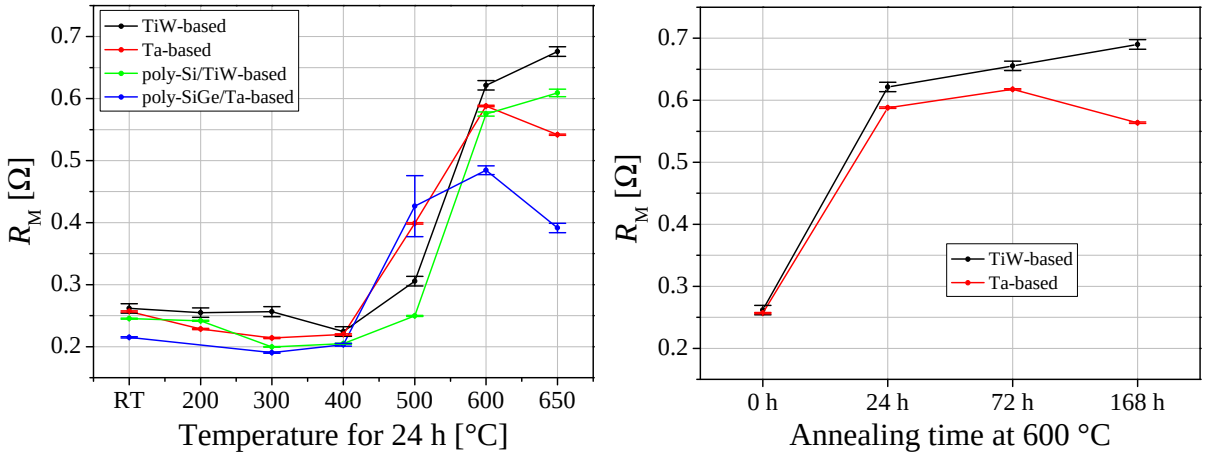


Figure 4.18: Change of R_{sh} due to annealing at given temperatures for 24 h (*left*) and for given time at 600 °C (*right*).

The decrease of R_{sh} from RT to400 °C could be due to the Ni layer recrystallization, which can be inferred from the XRD analysis. For the TiW-based barriers, a weak R_{sh} increase at 500 °C could be due to the insignificant interdiffusion between the Ni and TiW layers. A significant increase of R_{sh} at 500 °C for the Ta-based barrier was due to the early growth of the Ni_3Ta phase. After 600 °C annealing, both barriers exhibited approx. 3 times increase of R_{sh} due to the interdiffusion between the Ni and the TiW layers as well as the complete growth of the Ni_3Ta phase, which is determined in the XRD and TEM analyses. Moreover, they exhibited a slight R_{sh} change even after 650 °C annealing. After 600 °C annealing for 72 h, R_{sh} of the barriers, which were deposited on the *c*-Si substrate, increased slightly. After 168 h, the TiW-based and Ta-based barriers exhibited a slight increase and a slight decrease of R_{sh}, respectively.

4.2.5 Adhesion of the barriers

Adhesive tape test was performed before and after annealing on both barriers. Based on the classification in Figure 3.18, their adhesion was excellent and sufficient before and after annealing, respectively. This indicates that both barriers could still maintain their adhesion to the substrate after 600 °C annealing.

4.3 Ni-Sn bond solder

4.3.1 Ni-Sn electroplating

Thickness uniformity of the electroplated Ni structures

The thickness of an electroplated Ni structure was measured using a profilometer (AMBiOS Tech. XP-2 Profilometer) in order to investigate the capability of a pulsed current to deposit Ni structures with an enhanced thickness uniformity on a wafer. The electroplating was performed using a constant DC , a "1 s"-pulsed, and a "10 ms"-pulsed current. The achieved thickness non-uniformity as well as the electroplating parameters are given in Table 4.3. The Ni structure, which was electroplated using the pulsed current, has lower thickness non-uniformity in contrast to the electroplated Ni structure using the DC current. Although the thickness non-uniformity of the "10 ms"-pulsed current was higher than of the "1 s"-pulsed current, higher Ni structure thickness can be electroplated for a short duration using the "10 ms"-pulsed current in contrast to the thickness deposited using the "1 s"-pulsed current. Moreover, the "10 ms"-pulsed current can enhance the cathode efficiency of Ni electroplating.

Table 4.3: Thickness non-uniformities of three Ni electroplating methods based on the applied electrical current.

Methods	non-uniformities	Thickness	Duration	$a_{\text{eff.}}$	Seed layer
DC (1.6 A/dm²)	15 %	2.5 – 4.7 µm	30 min.	78 %	Au (150 nm) [94]
"1 s"-pulsed current*	6.4 %	2.7 – 3.7 µm	25 min.	67.2 %	Ni (100 nm)
"10 ms"-pulsed current**	7.9 %	3.0 – 4.0 µm	15 min.	85.5 %	Ni (100 nm), based on Section 3.2.3

*(5 mA (t_{OFF}) - 2 A/dm² (t_{ON})) **(i_{P}=3 A/dm² for 13 min.)

The Ni electroplating with milliseconds-pulsed current was performed by varying the applied current density I_ρ, duty cycle dc (t_{ON} and t_{OFF}), and time duration t_{TOTAL}. Table 4.4 shows the cathode efficiency $a_{\text{eff.}}$, the average height of the electroplated Ni structures, and the non-uniformity of the Ni structures thickness distributed over 6"-wafers. From the table, following can be summarized:

– The application of a high I_ρ (no. 1 and 2, no. 3 and 4) and a high dc (no. 4 and no. 5) could result in high $a_{\text{eff.}}$ and low thickness non-uniformities.
– The application of a low I_ρ with a high dc for a long t_{TOTAL} could result in a low thickness non-uniformity. However, the deposition rate could be low as well (no. 6).
– Electroplating using a low I_ρ for a short time at the beginning and then followed by high I_ρ (no. 9 – 13) was performed in order to suppress the reduction of the thickness non-uniformity within a short t_{TOTAL}. However, the thickness non-uniformities and the deposition rate seemed to remain the same (comparison between no. 5 and no. 7 – 10).

The "10 ms"-pulse plating was performed also to deposit the Ni structures on an 8"-wafer using a 100-nm-thick Ni layer as a plating base. Table 4.5 summarizes the thickness and the thickness non-uniformity of the electroplated Ni structure. Electroplating no. 1 results in a low Ni structure thickness in contrast to no. 2 because t_{TOTAL} of in no. 1 was shorter than in no. 2. Electroplating no. 1 in Table 4.5 results in a higher thickness non-uniformity than no. 7 in Table 4.4. This is rather due to surface preparation before electroplating, where the wafer's surface was not clean enough from a contamination and from an Ni native oxide. The measured

Table 4.4: Electroplating of a Ni layer using a milliseconds-pulsed current.

No.	"10 ms"-pulsed current			$a_{\text{eff.}}$ [%]	Thickness of Ni structures			
	I_ρ [A/dm²]	*dc*	t_{TOTAL} [min.]		Average [µm]		non-uniformity [%]	
					50 µm -wide	200 µm -wide	50 µm -wide	200 µm -wide
1	6.50	33	15	93.1	6.4	5.7	8.1	8.6
2	5.50	33	15	79.3	5.2	4.8	7.6	7.7
3	3.76	40	25	87.3	6.5	6.2	10.2	9.8
4	3.00	40	25	83.2	4.9	4.8	9.4	8.9
5	3.00	50	25	88.1	6.7	6.4	6.8	7.4
6	1.50	50	40	81.2	4.8	4.7	2.8	3.0
7	0.50	50	2	78.0	4.4	4.1	4.5	4.9
	1.50	50	4					
	3.00	50	14					
8	0.50	50	1	89.2	5.2	4.9	8.2	7.9
	1.50	50	1					
	3.00	50	18					
9	0.50	50	1	85.5	3.5	3.3	7.9	8.2
	1.50	50	1					
	3.00	50	13					
10	0.50	50	1	83.9	2.6	2.5	7.1	7.0
	1.50	50	1					
	3.00	50	10					

Table 4.5: Electroplating of a Ni layer using the "10 ms"-pulsed current with *dc* = 50% on 8"-wafers.

No.	I_ρ [A/dm²]	t_{TOTAL} [min.]	Thickness of Ni structures			
			Average [µm]		non-uniformity [µm]	
			Large	Small	Large	Small
1	0.20	2	4.2	4.6	10	9.1
	0.50	4				
	0.80	14				
2	0.20	1	5.3	5.6	4	3.7
	0.50	1				
	0.80	18				

$a_{\text{eff.}}$ should be similar to Ni electroplating using the 6"-wafer, because the deposition rates are ~0.23 µm/min and ~0.27 µm/min for electroplating no. 1 and no. 2, respectively, which are similar with the deposition rate of no. 7 and no. 8 in Table 4.4.

Figure 4.19 shows the SEM images of a surface and a side wall of an electroplated Ni

structure deposited using the "10 ms"-pulsed current. If one compares the Ni structure surface between the top-right and the bottom-right SEM images, it can be approximated that the roughness is below 1 µm. Using a profilometer, the surface roughness of the Ni structure was determined <40 nm for electroplating using both "1 s"-pulsed and "10 ms"-pulsed currents.

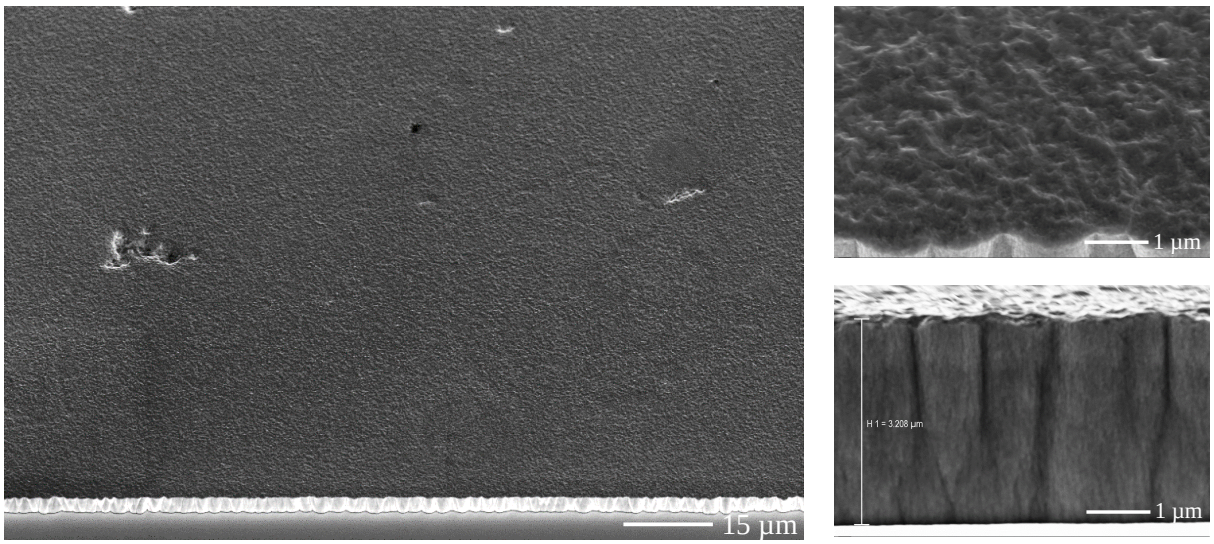


Figure 4.19: SEM images of a surface (*left* and *right-top*) and a side wall (*right-bottom*) of the Ni structure electroplated using the "10 ms"-pulsed current.

Surface roughness of the electroplated Sn structures

The surface roughness *Ra* of an electroplated Sn structure was measured in order to investigate the capability of the pulsed current in depositing a layer having a low *Ra*. Electroplating with the DC current could had achieved *Ra* ≈2.0 µm [94]. With the pulse plating, it can be as low as *Ra* = 131 nm and *Ra* = 469 nm for electroplating using the "1 s"-pulsed and "10 ms"-pulsed currents, respectively, as depicted in Figure 4.20-*left*. Moreover, the pulse plating using the

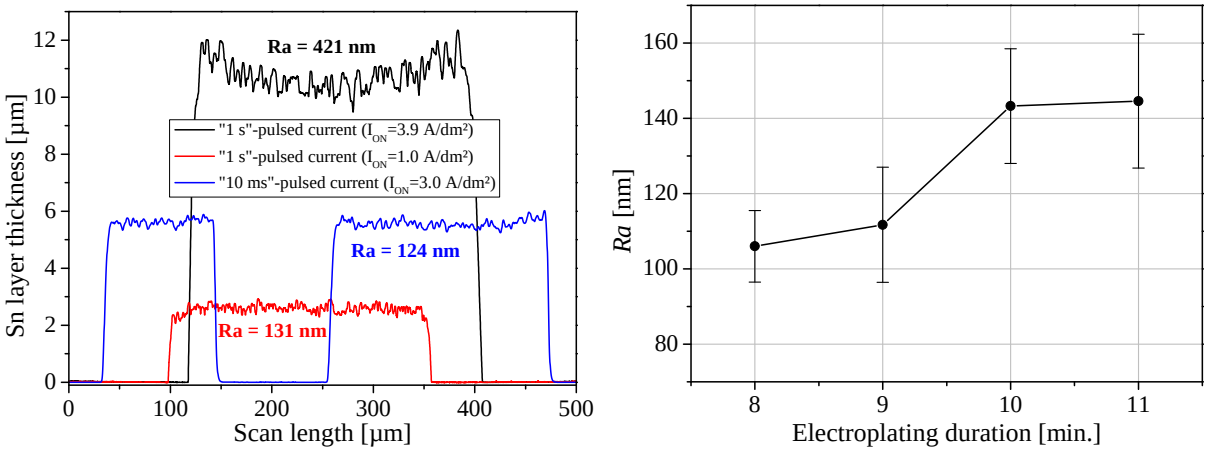


Figure 4.20: Thickness profiles of three Sn structures electroplated using a pulsed current (*left*) and the averages of *Ra* for given electroplating durations (*right*). The Sn structure, which was electroplated using the "10 ms"-pulsed current, was deposited on an ~2.5-µm-thick Ni structure. The averages of *Ra* were taken from measurements on a 200-µm-wide Sn structure at 21 locations over a wafer.

"1 s"-pulsed current could deposit an ~11-µm-thick Sn structure having *Ra* = 421 nm using a high I_ρ for 15 min. As shown in Figure 4.20-*right*, *Ra* depends on t_{TOTAL}. Electroplating with t_{TOTAL} = 11 min. have a similar *Ra* to electroplating with t_{TOTAL} = 10 min. This indicates that the application of the pulsed current in electroplating for a longer duration could maintain a low *Ra* with a high structure thickness. From 30 times of electroplating, the average of the deposition rate and $a_{\mathrm{eff.}}$ was 0.28 nm/min and 77.8 %, respectively. Figure 4.21 shows two SEM images of an electroplated Sn structure deposited using the "1 s"-pulsed and "10 ms"-pulsed currents, where their surfaces show a similar profile. Comparing with the previous work [94], the pulse plating modified the appearance of the Sn layer from satin bright to matte.

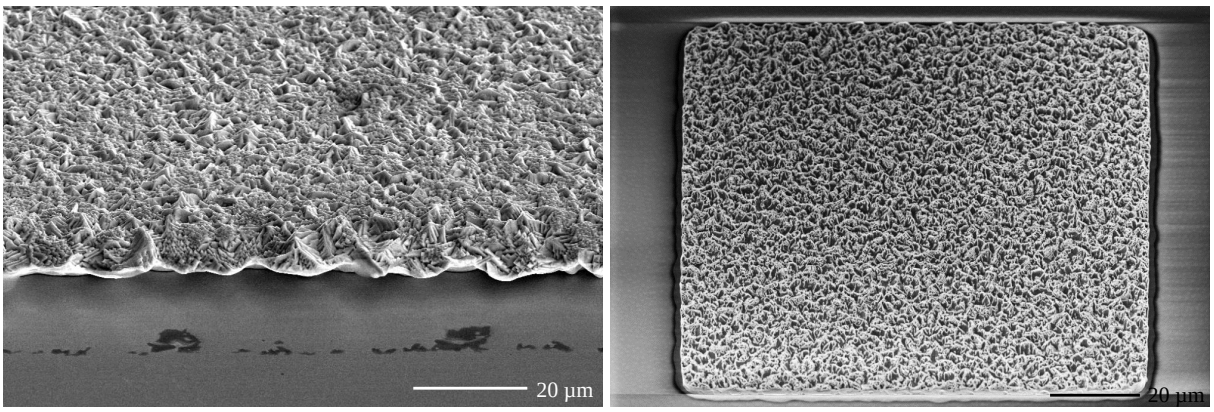


Figure 4.21: SEM images of a Sn structure electroplated using the "1 s"-pulsed (*left*) and "10 ms"-pulsed (*right*) currents.

4.3.2 Ni-Sn TLP wafer bonding

A number of the Ni-Sn TLP wafer bonding, which is listed in Table 3.3, was performed to investigate the property of the bond solder (Ni-Sn IMC layer) in regards to the bond time, the bond pressure, and the thickness of the Ni and Sn layers. A typical cross-section of an Ni-Sn TLP bond solder is shown in Figure 4.22-*top*, where distinct interfaces (2 interfaces with 3 layers) within the bond solder can be observed clearly after wafer bonding. The compound of the layers was determined using the EDX analysis, which is summarized in Table 4.5. On both sides of the bond solder, residual of Sn remains unreacted on the surface. After wafer bonding, the misalignment between the top and the bottom wafers was determined. All wafer bonding has <15 µm of a misalignment, except wb-C has ~25 µm of a misalignment.

Wafer bonding with a short bond time

Wafer bonding with 60 min, 30 min and 15 min of a bond time was performed in order to investigate the effect of the bond time to the element concentration of the bond solder. The investigation employed an EDX point measurements, which was performed at three locations on a bond solder cross-section. Table 4.6 summarizes the investigation at three locations indicated on the accompanied SEM image.

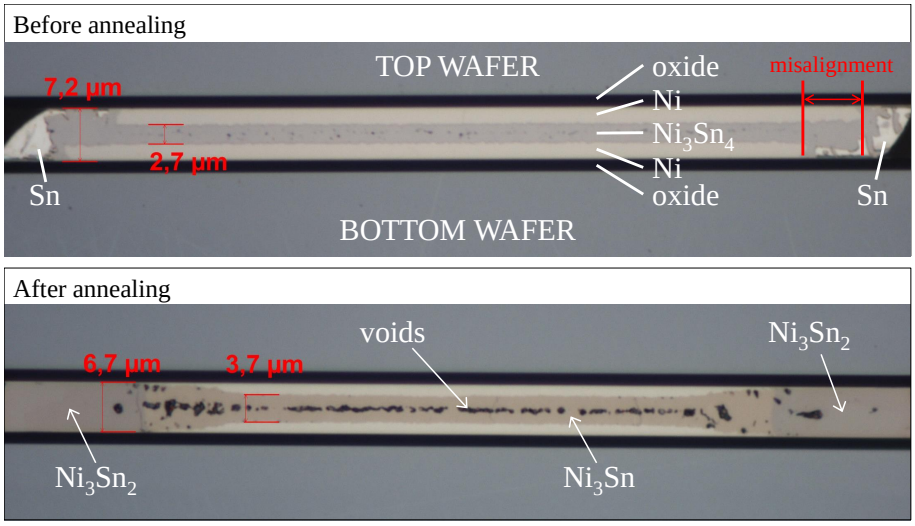
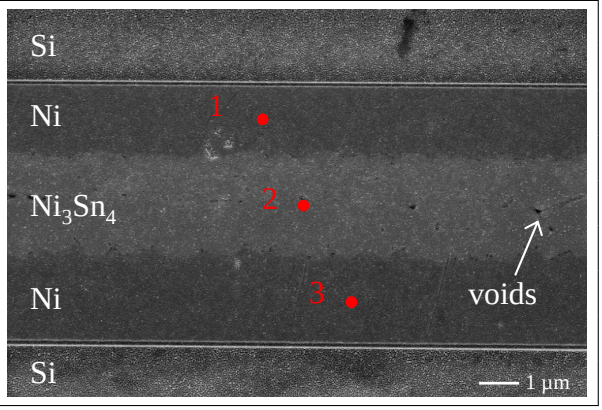


Figure 4.22: Light microscope images of a typical Ni-Sn TLP bond solder cross-section before (*top*) and after (*bottom*) annealing. The images were taken from a structure with $100 \times 100\,\mu m^2$ of size, which was fabricated using wafer bonding with 15 min of a bond time and 0.5 bar of a bond pressure. The indicated layers were determined using the EDX analysis.

Table 4.6: Atomic concentrations from three locations indicated on the cross-sectional SEM image of a bond solder before annealing. Three non-annealed bond solder fabricated using 60 min, 30 min and 15 min of a bond time were taken for EDX point measurement.

wb-	Ni-Sn	at.% of Ni and Sn		
		Locations		
		1	2	3
A 60 min.	Ni	99.9	46.5	99.8
	Sn	0.1	53.5	0.2
C 30 min.	Ni	96.4	64.4	99.6
	Sn	2.7	34.3	0.4
F 15 min.	Ni	98.5	46.4	98.9
	Sn	0.6	53.6	0



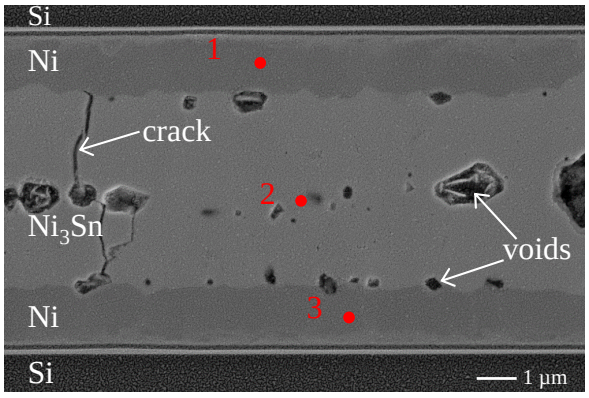
Location 1 and 3 for three wafer bonding exhibit a high concentration of Ni atoms. This indicates that the layers belong to the electroplated Ni structure, which had not been reacted with Sn atoms during wafer bonding. At location 3, the Ni-Sn concentration shows a Ni_3Sn_4 phase for wb-A and wb-F, and a Ni_3Sn_2 phases for wb-C. As depicted on the accompanied SEM image of the bond solder cross-section of wb-F, voids with ~100 nm of diameter were observed within the Ni_3Sn_4 layer due to an organic contamination on the Sn surface before wafer bonding.

The impact of annealing to the bond solder

Three distinct interfaces can still be observed on the bond solder cross-section after annealing as depicted in Figure 4.22-*bottom*. The Ni_3Sn_4 layer was transformed to a Ni_3Sn layer having a thick layer followed with voids formation within this layer. The Sn residues reacted with Ni atoms resulting in growing of the Ni_3Sn_2 phase (59.8 at % and 40.2 at % of Ni and Sn, respec-

Table 4.7: Atomic concentrations from three locations indicated on the cross-sectional SEM image of a bond solder, which was annealed at 600 °C for 24 h. Three annealed bond solder fabricated using 60 min, 30 min and 15 min of a bond time were taken for EDX point measurement.

wb-	Ni-Sn	at.% of Ni and Sn		
		Locations		
		1	2	3
A 60 min.	Ni	99.8	73.9	99.7
	Sn	0.2	26.1	0.3
C 30 min.	Ni	78	74.8	93.6
	Sn	21	24.2	6.4
F 15 min.	Ni	95.8	77.4	98.1
	Sn	3.4	21	1.8



tively), which broadened the bond solder width, and narrowed and thinned the Ni layers on both sides.

The effect of annealing on bond solders fabricated with three different bond times was investigated. The investigation employed point measurements of the EDX analysis, which was performed at three locations on an annealed bond solder cross-section. Table 4.7 summarizes the investigation at three locations indicated on the accompanied SEM image of wb-F after 600 °C annealing. Location 1 and 3 have a high Ni concentration indicating that the Ni layers were still not reacted with Sn atoms completely. The thickness of the deposited Ni structures in wb-C was 1.7 µm, which was thin enough to have a thin unconsumed Ni layers (~0.5 µm) after annealing (see Figure 4.27. This thickness leads to a strong interaction volume effect in the EDX analysis. Location 2 has a similar Ni-Sn concentrations among three wafer bonding that the broadening layer was determined having the Ni_3Sn phase. Large voids with >1 µm of diameter are observed within the Ni_3Sn layer as well as on the interface between the Ni and Ni_3Sn layers. Layer cracks, which could be due to a high layer stress, were also observed within the Ni_3Sn layer.

Voids in the Ni_3Sn layer of a daisy chain structure after annealing

Wafer bonding was performed with different bond pressures in order to produce a thick Ni_3Sn_4 layer, which was intended not to let the voids formed after annealing. However, large voids were still observed after annealing for all wafer bonding with the different Ni_3Sn_4 layer thicknesses. An interesting observation can be seen in Figure 4.23-*top*, which shows an annealed bond solder of a daisy chain structure having a less content and smaller size of voids within the Ni_3Sn layer in contrast to the voids in the structure with $100 \times 100\,\mu m^2$ of size. However, if the Ni layer is electroplated too thin for the daisy chain bond solder, for example 1.7 µm in wb-C, then a significant void formation will be exhibited within the Ni_3Sn layer after annealing as depicted in Figure 4.23-*bottom*.

4.3.3 Bond stability investigation

As depicted in Figure 4.24-*left*, the bond strengths of the bond solders produced using different parameters of wafer bonding (see Table 3.3) exhibit a higher bond strength than the minimum

bond strength (24.8 MPa, see chapter 3.3.9), before and after annealing. The bond solder fabricated using 15 min and 30 min of a bond time has a higher bond strength than using 60 min of a bond time. However, this bond time dependency should be analyzed further by taking into account the break analysis depicted in Figure 4.24-*right*, which provides more information in investigating the quality of a bond solder.

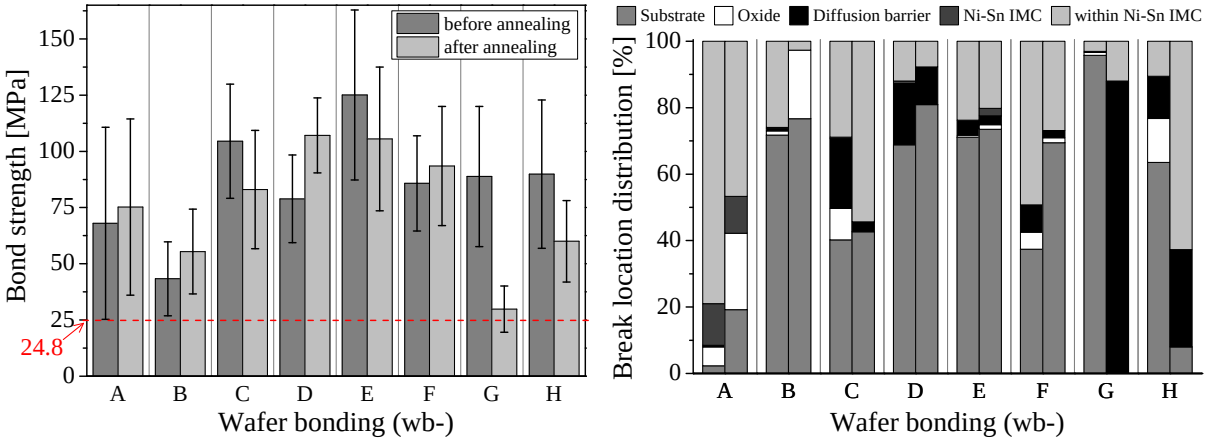


Figure 4.24: Bond strength (*left*) of bond solders fabricated using eight wafer bonding with different bonding parameters and break location distribution (*right*) from several shear-tested bond solder. Two bars in a wafer bonding correspond to before (left bar) and after (right bar) 600 °C annealing.

In wb-A and wb-F, most of the break is occurred within the Ni-Sn IMC layer before annealing in contrast to other wafer bonding due to a significant void formation within the Ni_3Sn_4 layer. However, the break distribution within the Ni-Sn IMC layer in wb-F is lower than in wb-A because the void formation significance in wb-F was not as strong as in wb-A. Voids can be significantly formed if the surface interlayer (Sn layer) was not prepared well before wafer bonding. A poor surface preparation would let the contamination, such as an organic residual from an incomplete resist stripping, remains on the surface. After annealing, the break distribution within the Ni-Sn IMC layer decreased but the bond strength was approximately unchanged indicating that the bond solder strengthened its bond stability. This results in increasing the

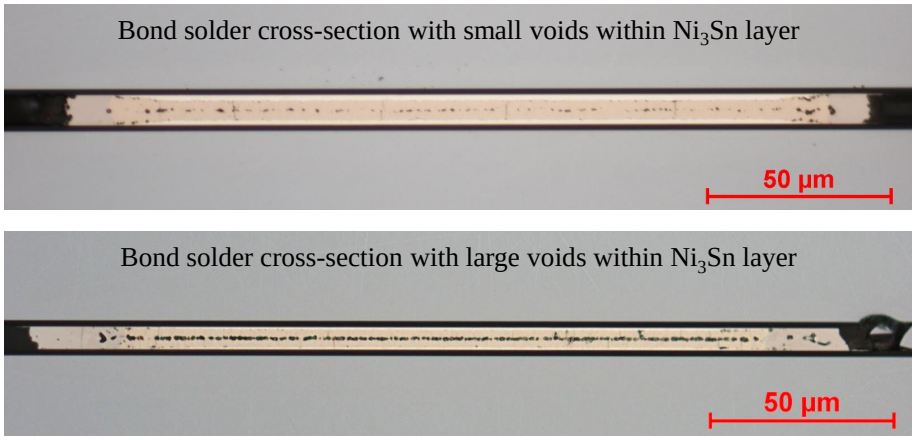


Figure 4.23: Light microscope images of a bond solder cross-section taken from a daisy chain structure after annealing. The wafer bonding for each image were from wb-F (*top*) and wb-C (*bottom*).

distribution of a break location on the oxide (only in wb-A) and within the Si substrate.

In wb-B, wb-D, and wb-E, most of the break occurred mostly within the Si substrate before and after annealing showing that the bond solder exhibits a high thermal stability. This determination is observed as well from the bond solder for wb-G and wb-H before annealing. However, the bond strength in wb-B is not as high as in wb-D and wb-E because the Si substrate in wb-B has a poor stability.

In wb-C, there is ~20 % of a break distribution where the barrier is delaminated indicating a poor adhesion of the barrier on the oxide. There is also ~29 % of a break within the Ni-Sn IMC layer due to a significant misalignment (~33 µm) between the top and the bottom wafers. After annealing, more than 50 % of a break distribution within the Ni-Sn-IMC layer due to the misalignment and the void formation. However, the bond solder before and after annealing exhibited a higher bond strength than in wb-B indicating a high mechanical stability of the bond solder despite of the poor adhesion, the apparent misalignment, and the void formation.

In wb-G, a significant decrease of the bond strength after annealing is due to the weakening of the barrier stability, which can be indicated from a high break distribution of the barrier delamination. Figure 4.25-*left* shows the break of a bond solder due to the shear test after annealing in wb-G, where ~50 % of bond structures are broken within the bond solder and another ~50 % is the barrier delamination (at the interface between the Ta and the TiN layers). In Figure 4.25-*right*, the barrier delamination is observed that the TiN layer is delaminated from the Ta layer, which is adjoined to the Si substrate. The wide-adjusted focus between the top and the bottom images in Figure 4.25-*right* indicates that a part of the bond solder structures are not broken due to the shear test but it is delaminated at the interface between the Ta and TiN layers, either from the top or bottom Si substrate. The delamination at the interface between the Ta and TiN layers could be caused by the stress relaxation, which is determined in the XRD analysis of the Ta-based barrier after 600 °C annealing, of the Ta layer, which is adjoined to the Si substrate.

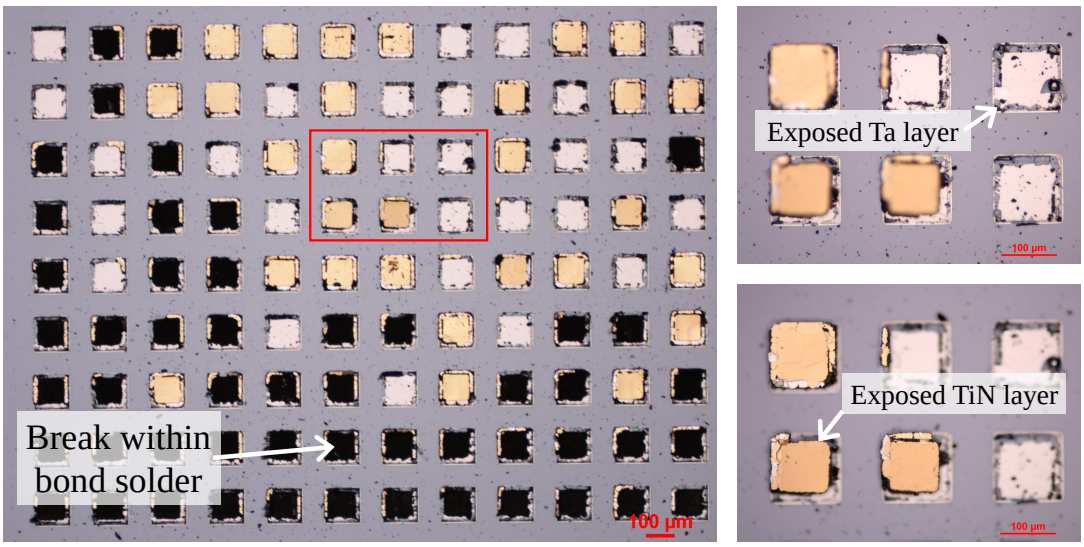


Figure 4.25: Top view of the annealed bond solder of wb-G after the shear test. The red rectangle emphasizes the six bond solder, which is magnified at the right side. The magnification images are focused at the Ta (*top*) and TiN layers (*bottom*). The barrier was Ta-based. Yellow surface indicates that the surface belongs to the TiN layer.

The delamination caused by the stress relaxation of the Ta layer was also encountered in wb-H, however, the bond strength in wb-H was not as low as in wb-G after annealing indicating

that the weakening of the barrier stability in wb-H was not as strong as in wb-G. Most of the break in wb-H occurred within the Ni-Sn IMC layer after annealing due to a significant void formation.

4.3.4 Electrical stability investigation

The average electrical resistance R_M of a daisy chain structure fabricated in 6 wafer bonding is shown in Figure 4.26. After annealing, R_M increases with varied differences for each wafer bonding.

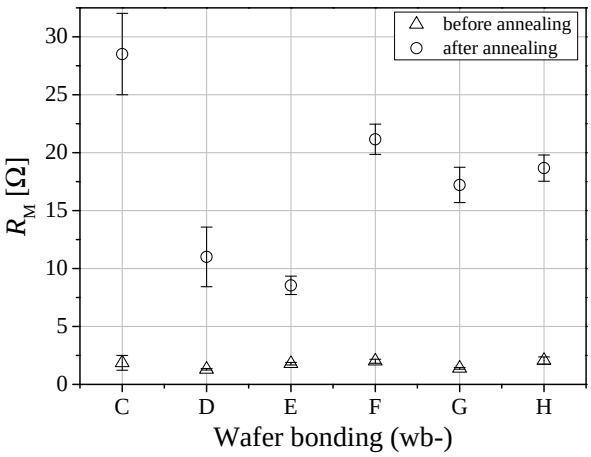


Figure 4.26: Average value of R_M of daisy chain structures before and after annealing.

In order to investigate R_M of a daisy chain structure before and after annealing thoroughly, the thicknesses of the Ni, Ni_3Sn_4, and Ni_3Sn layers were measured using a light microscope and then they were plotted together with R_M as depicted in Figure 4.27. Before annealing, R_M depends strongly on the thickness of the unconsumed Ni layer that R_M is approximately inversely proportional to the Ni layer thickness. However, although the daisy chain in wb-C has the thinnest Ni layer, it exhibits a low R_M due to the high Ni concentration (see Table 4.5) within the Ni_3Sn_4 layer. After annealing, the dependency of the Ni_3Sn layer thickness to R_M is became pronounced although it is not as high as the dependency on Ni layer thickness.

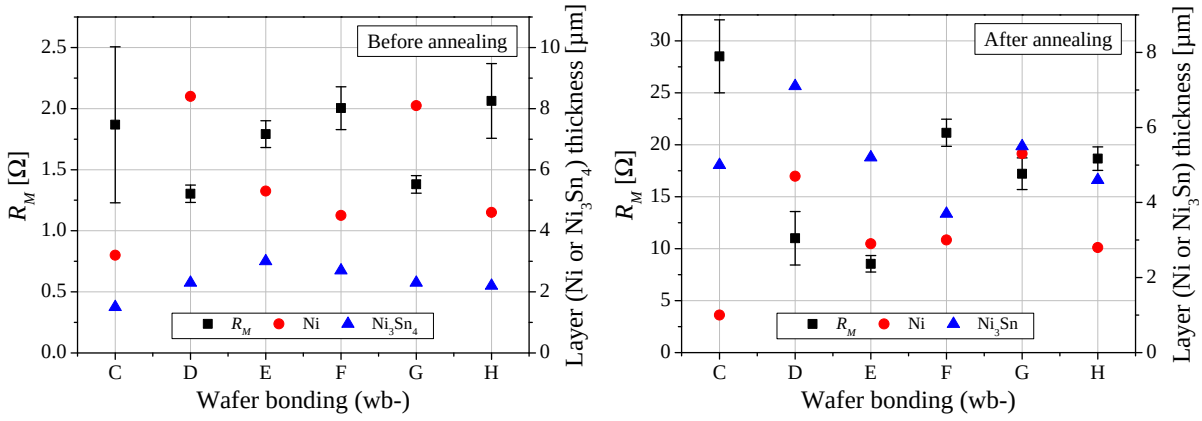


Figure 4.27: Dependency of R_M due to the layer thickness within the bond solder.

4.4 Transfer length measurement

4.4.1 Measurement on TLM structures with the TLM Au pads

A typical TLM plot for determining sheet resistance R_{sh} and contact resistivity ρ_C is shown in Figure 4.28. After linear fitting of R_M, the fitting line has a slope = 0.087 and intercepts on x-axis at –g = 137.6. Using Equation 2.7 and 2.8, it can be determined that R_{sh} and ρ_C equal 26.1 Ω and 1.2×10^{-3} Ω·cm^2, respectively.

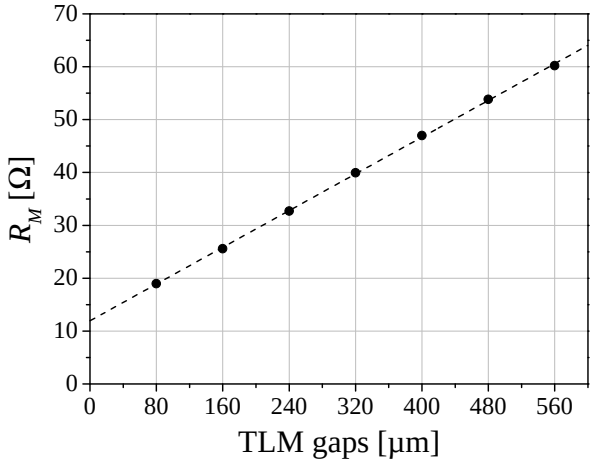


Figure 4.28: Plot of R_M and its dashed fitting line from a TLM structure having G80 of a TLM gap type and 300 μm of a TLM pad's width. The number (10, 20, 40, 60, and 80) of the TLM gap types corresponds to the smallest spacing in micrometer between the first and the second TLM pads (see Figure 3.5 for the detail).

The determined R_{sh} and ρ_C after TLM fabrication for both barriers show a variation indicated by error bars as depicted in Figure 4.29 and 4.30. The variation in R_{sh} is <10 % for G20, G40, G60, and G80 of TLM Gap types but it is higher for G10 because the accuracy in fabricating an ideal TLM structure is became more sensitive as the TLM gap becomes narrower. Figure 4.31 shows this fabrication sensitivity, where two TLM pads are close to each other due to an over-development of a photoresist and a steep Au layer's wall. For the TLM5 structure, R_{sh} is slightly stable for G40, G60, and G80. It increases for G20 and more in G10 because the first two TLM pads shown in Figure 4.31 are so close that the barrier within this gap could had not been etched away resulting in a low R_M thus a high slope of the fitting line is obtained.

It can also be observed in Figure 4.29 that the wider the TLM pad's width, the higher is R_{sh}. This relation shows that the width Z has a high significant effect on R_{sh}. This dependency is also observed in ρ_C as depicted in Figure 4.30 that Z or the TLM pad area gave a significant effect on the measured ρ_C [110]. The variation in ρ_C is above 10 % that can be related to inhomogeneous material properties, such as the thickness variation of electroplated Au and the chemical structure non-uniformity of the barriers over a wafer's surface. The thickness variation of the electroplated Au was in the range of 10–20 %. The gradual decrease of barrier's surface glazing was observed from the wafer's center to the wafer's edge indicating a chemical property non-uniformity of the deposited barrier. It can also be observed that ρ_C for each Z is higher in TLM10 than in TLM5. This difference is due to the clearance from the TLM pads to the poly-Si layer's edge in TLM10 that the electric current flows around the clearance into the pads leading to the increase of the measured voltage [110].

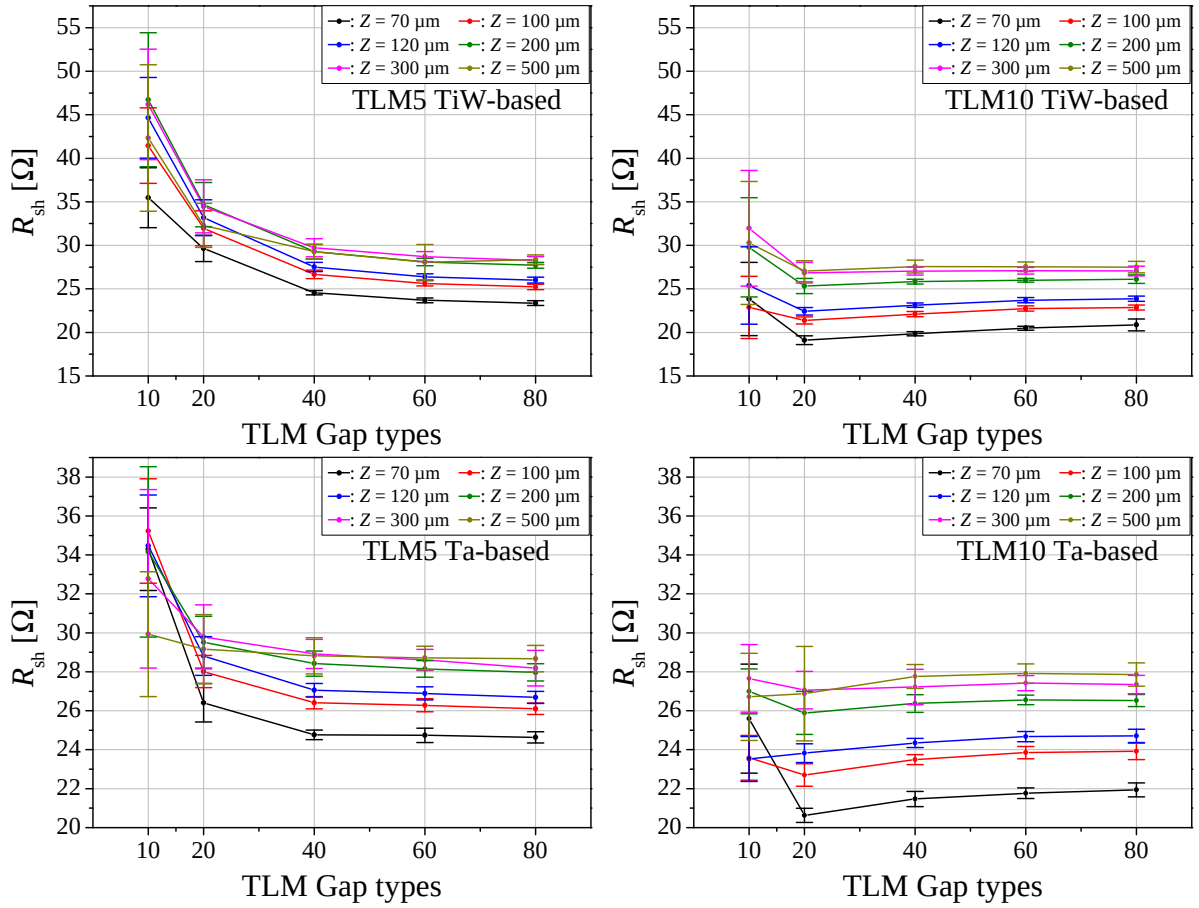


Figure 4.29: Sheet resistance R_{sh} after the fabrication of the TiW-based (*top*) and Ta-based (*bottom*) barriers. The numbers; 5 and 10 in TLM5 and TLM10, are corresponded to the distance between TLM pad's edge and poly-Si layer's wall; 5 µm (TLM5) and 10 µm(TLM10). See Figure 4.31-*left*

After annealing, R_{sh} shows a gradual increase up to 600 °C annealing for both barriers as depicted in Figure 4.32, except for the Ta-based barrier with TLM5 where R_{sh} decreases slightly. The gradual R_{sh} increase can be related to the induced layer stress within the poly-Si layer that has more profound effect at higher temperatures. The slight R_{sh} decreases may be caused from the Au diffusion, which is evidence from the TEM analysis, that was already took place and has given an additional conductivity into the poly-Si layer. Figure 4.32-*left* shows the Au diffusion on the poly-Si surface. For TLM5 with G10 and G20 (see also Figure A.8 and A.9 in Appendix), R_{sh} increases significantly due to the fabrication sensitivity in a smaller TLM structure. After 650 °C annealing, R_{sh} cannot be measured on TLM5 due to a significant alteration of the poly-Si layer as shown in Figure 4.32-*right*. At this annealing temperature for TLM10, only a small number of TLM structure can be measured, therefore R_{sh} is scattered greatly.

After annealing, ρ_C shows a slight increase up to 500 °C annealing for TLM5 in both barriers as depicted in Figure 4.34-*left* as well as in Figure A.10 and A.11. This slight increase can be related to the interdiffusion between the Ni and the adjoining TiW and Ta layers for the TiW-based and Ta-based barriers, respectively. Up to 500 °C annealing, TLM10 shows a higher ρ_C than TLM5 due to the current flow, which is around Au pads since the distance between the TLM pad and the poly-Si layer's edge is visible. After 600 °C annealing for the TiW-based barrier and TLM5, ρ_C is approximately stable for $Z \leq 120$ µm and increases slightly

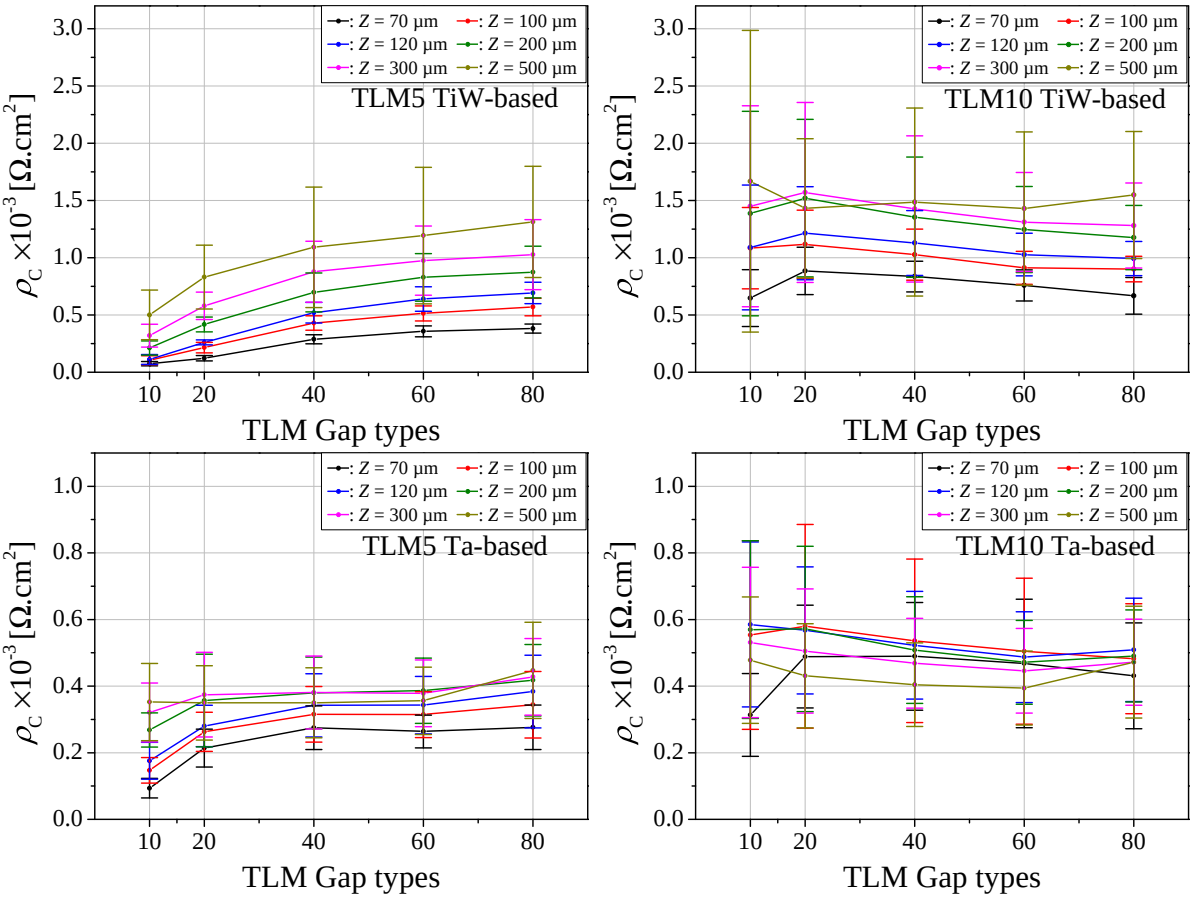


Figure 4.30: Contact resistivity ρ_C after the fabrication of the TiW-based (*top*) and Ta-based (*bottom*) barriers.

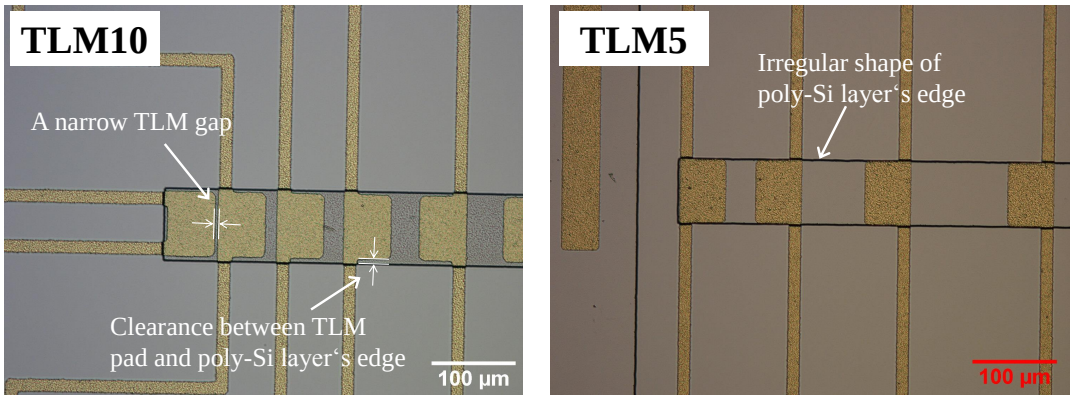


Figure 4.31: TLM structures of TLM10 with G10 (*left*) and TLM5 with G40 (*right*) before barrier removal. It is measured that the clearance from the TLM pads to the poly-Si layer's edge is <10 µm for TLM10 and almost zero for TLM5. The latter is favorable for a TLM measurement [110].

for Z >120 µm. Higher ρ_C in larger TLM pads rather than in smaller TLM pads can be caused by the influencing factors (see Chapter 2.3), which become more profound in larger TLM pads than in smaller TLM pads. For the Ta-based barrier and TLM5, ρ_C decreases slightly that can be related to the Au diffusion, which reduces the resistivity of the poly-Si layer, and it was failed for being measured for G10 and G20 due to the significant alteration of the poly-Si layer. After

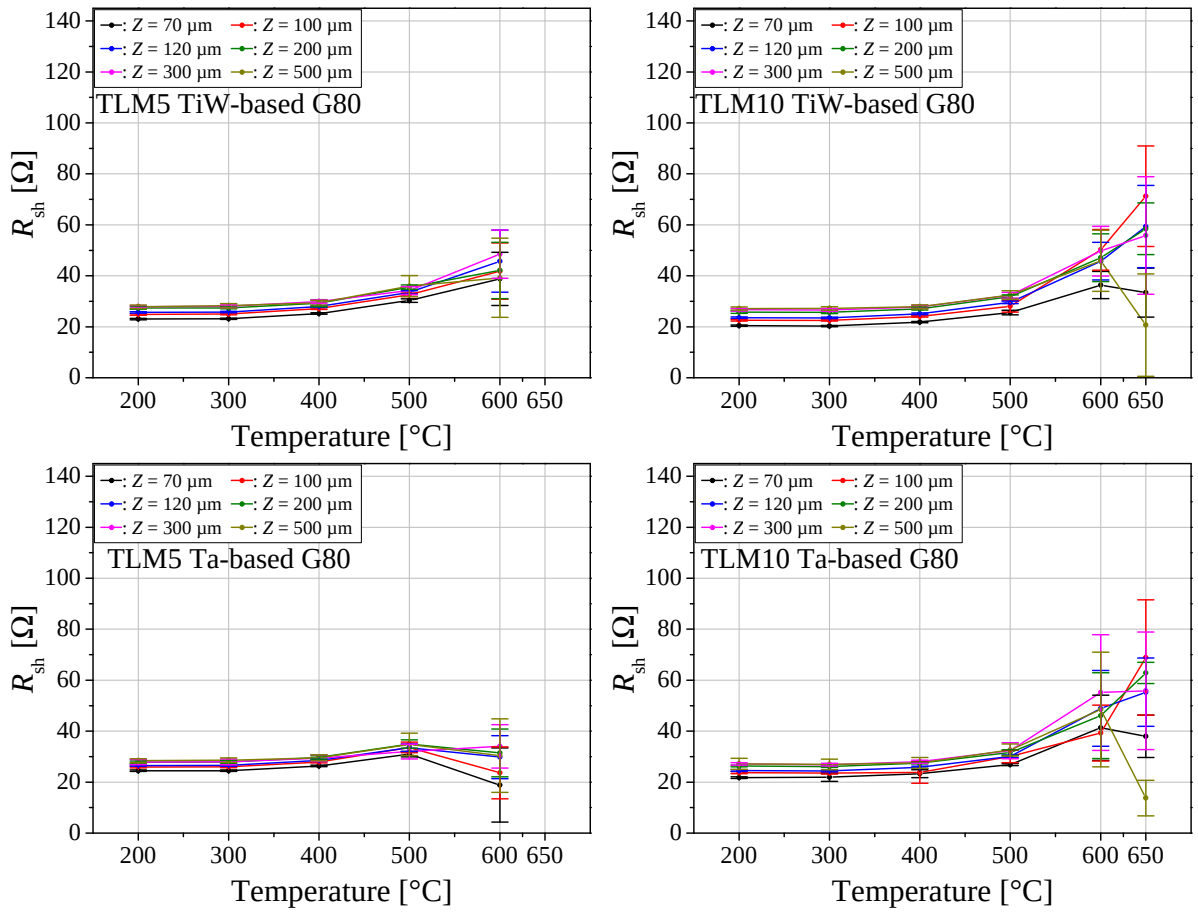


Figure 4.32: Sheet resistance R_{sh} after annealing of the TiW-based (*top*) and Ta-based (*bottom*) barriers. For plots of G10, G20, G40, and G60, see Appendix.

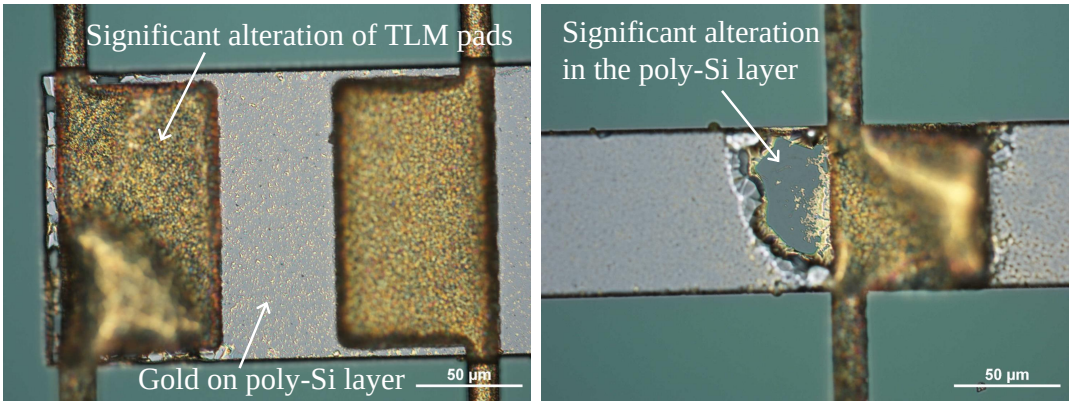


Figure 4.33: Structural alteration after 600 °C annealing in both barriers: a Au diffusion into the poly-Si layer *left* and a significant alteration of the poly-Si layer *right*.

600 °C annealing for both barriers and TLM10, ρ_C increases significantly due to a significant alteration of the TLM pads microstructure as shown in Figure 4.32-*left*. After 650 °C annealing, ρ_C was failed for being measured due to the significant alteration of the poly-Si layer for both barriers with TLM5. For both barriers with TLM10, ρ_C decreases and cannot be measured in a number of the TLM structure due to the the Au diffusion and the significant alteration of the poly-Si layer.

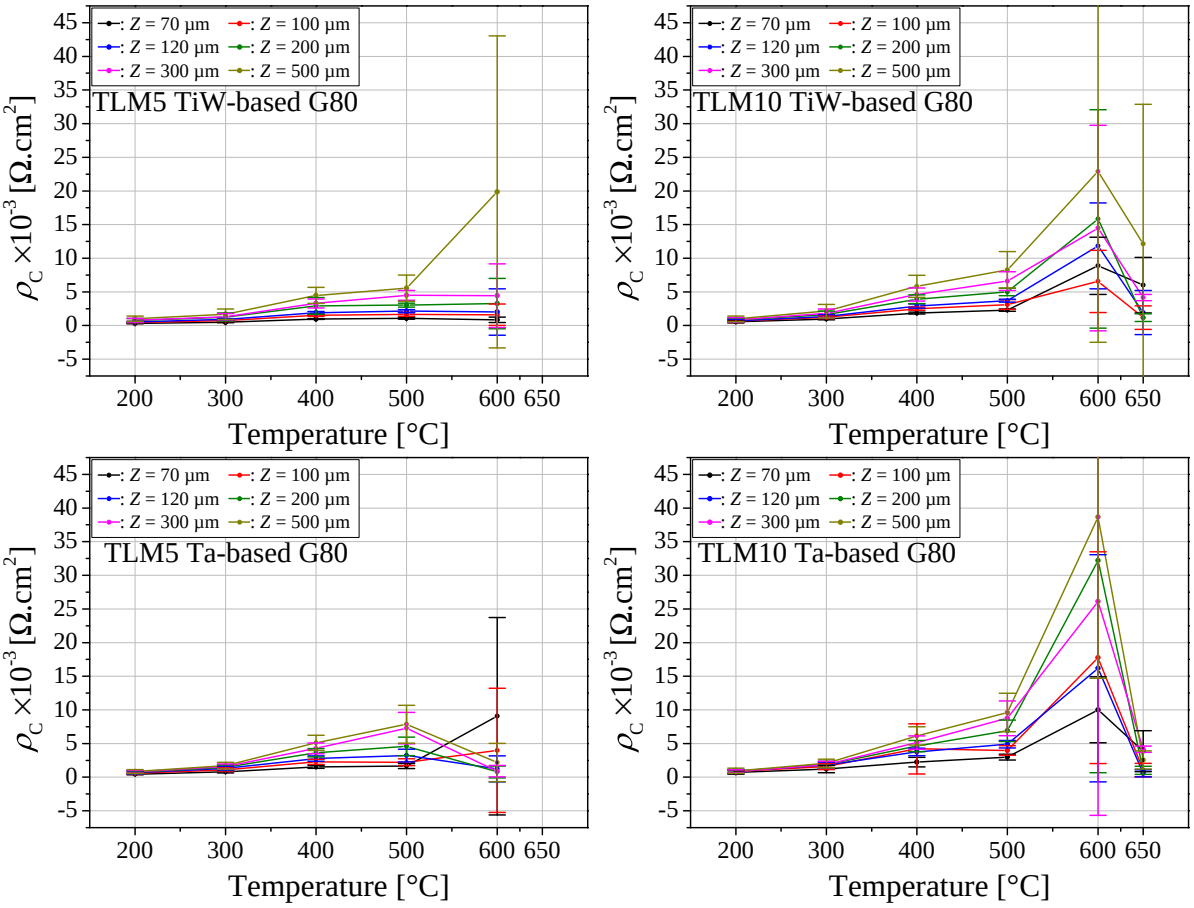


Figure 4.34: Contact resistivity ρ_C after annealing of the TiW-based (*top*) and Ta-based (*bottom*) barriers. For plots of G10, G20, G40, and G60, see Appendix.

4.4.2 Measurement on TLM structures without the TLM Au pads

This measurement was dedicated to determine R_{sh} and ρ_C by eliminating the effect of Au pads at all given annealing temperatures. It is shown from the TEM analysis that if Au is not present on the top of the barriers, then no material diffusion is determined into the poly-Si layer after 600 °C annealing. Before annealing, it is determined that R_{sh} = 31.3 ± 1.0 Ω and ρ_C = 1.11 ±

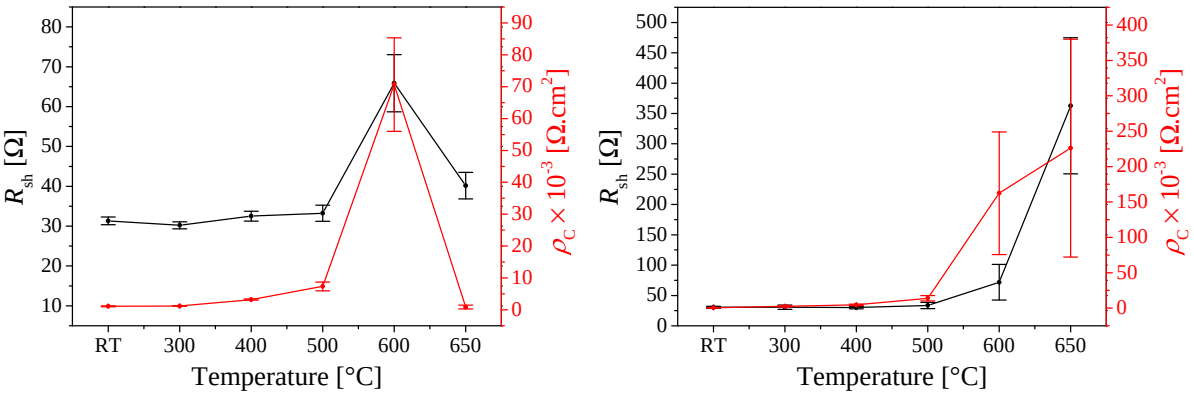


Figure 4.35: Increase of R_{sh} and ρ_C determined from the TLM measurement at given annealing temperatures for the TiW-based (*left*) and Ta-based (*right*) barriers. The inset is to show R_{sh} in detail.

0.130 mΩ·cm² for the TiW-based barrier. It is determined that R_{sh} = 30.7 ± 1.7 Ω and ρ_C = 0.61 ± 0.25 mΩ·cm² for the Ta-based barrier. Comparing these values with the values shown in Figure 4.29 and 4.30 shows that R_{sh} is higher than for the measurement with the TLM Au pads and ρ_C is in the range of values for the measurement with the TLM Au pads. The increase of both parameters due to annealing is shown in Figure 4.35. From RT to 500 °C of annealing temperature, R_{sh} remains approximately constant and ρ_C increases slightly. This indicates no material diffusion into the poly-Si layer and the barriers could be induced by a tensile stress during annealing.

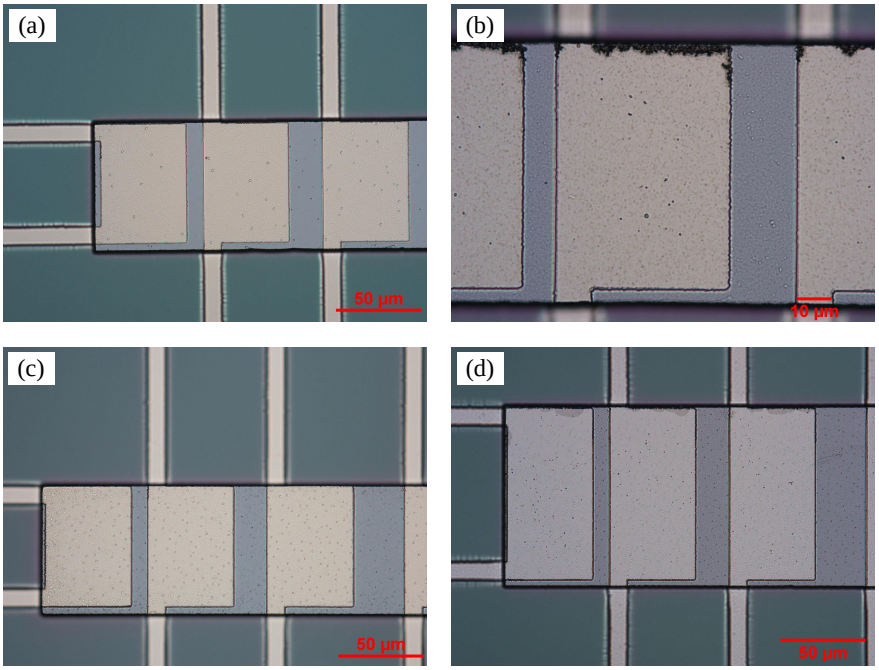


Figure 4.36: Top view of TLM pads without an electroplated Au layer for the TiW-based (a, b) and Ta-based (c, d) barriers before (a, c) and after 600 °C annealing (b, d).

After 600 °C annealing, both barriers exhibit R_{sh} increase >100 % because the poly-Si layer was induced by the tensile stress that has more profound effect. The significant increase in ρ_C could be caused by the interdiffusion between the Ni and the adjoining TiW layers for the TiW-based barrier and by the Ni_3Ta growth for the Ta-based barrier. The strong significance of the ρ_C increase in the Ta-based barrier could be due to the stress relaxation of the Ta layer adjoined to the Si substrate. The decrease and the increase of R_{sh} and ρ_C for the TiW-based and Ta-based barrier, respectively, after 650 °C annealing cannot be investigated because there is no evidence to support the analysis.

Figure 4.36 shows the surface of TLM pads and the poly-Si layer after 600 °C annealing, where insignificant alteration can be observed on the surface and on the edge of the TLM pads due to the interdiffusion between the Ni and the adjoining TiW layer for the TiW-based barrier and between the Ni and the adjoining Ta layers for the Ta-based barriers.

Chapter 5

Discussion

In this chapter, the interpretation of the results is presented and discussed. The TiW-based and Ta-based barriers were deposited by stacking thin films on an 8"-wafer in each type, and were investigated for high temperature reliability up to 600 °C. The investigation was performed before and after annealing at given temperatures for 24 h. The investigation included an XRD analysis, a TEM analysis, a 4-probe sheet resistance measurement, and an adhesion tape test. The Ni-Sn TLP bond solder was fabricated in order to create an IMC which is stable at high temperature up to 600 °C. The stability was determined by the shear test and the electrical resistance change of the daisy chain structures. The TLM structures were fabricated in order to determine the contact resistivity between each barrier and poly-Si layer. The high temperature stability of the contact resisitivity was also investigated. The purpose of these investigations was to develop a stable and reliable metallic joint, which can be integrated in a μTEG operated at high temperature.

5.1 Stress compensation

The barriers were deposited thick in order not to let material diffuse into the Si substrate. However, a thick barrier can exhibit a high tensile or compressive stress that leads to a significant wafer curvature, which is problematic in the wafer processing, especially in the lithography. A thin film of TiW or Ta can be used as a diffusion barrier and it exhibits a tensile stress after deposition. A thin film of TiN exhibits a compressive stress after deposition and therefore can be sandwiched by two TiW layers or by two Ta layers in order to compensate the final stress after the TiW-based and Ta-based barriers are fabricated as indicated in Table 4.1. Sandwiching of the TiN layer may also be advantageous because nitrogen does not diffuses into the adjoining Ta layers after 600 °C annealing as determined in the EFTEM analysis. This result is better than if a TaN thin film is sandwiched by two Ta layers as reported in a published study [50]. This improvement can be analyzed from the standard enthalpy of formation ($\Delta_f H^0$) at 600 °C, where a TiN compound has a lower enthalpy ($\Delta_f H^0$ TiN = −325 kJ/mol) than the enthalpy of TaN ($\Delta_f H^0$ TaN = −273 kJ/mol) or Ta_2N ($\Delta_f H^0$ Ta_2N = −250 kJ/mol) compounds [122]. Since a chemical reaction of a compound formation is established preferably in a reaction that requires the lowest enthalpy, the TiN layer has higher chemical stability than TaN or Ta_2N layers, therefore nitrogen will not diffuse into both Ta layers. The application of a Ni layer instead of a Au layer as a top layer was useful for a plating base of a TLP bond solder deposition. This is discussed in Section 5.5.

5.2 Determination of phases

The XRD analysis was performed in order to determine whether compounds between the barrier's elements and the Si substrate (silicides) were grew by observing 2θ peaks of silicide phases. The silicides' growth can be an indication of a material diffusion into the Si substrate. From RT to 600 °C annealing, no silicides were determined in either barriers. The silicides did not grow as the barriers deposited either on the *c*-Si substrate or on the poly-Si(Ge) substrates. New phases between the Ni and TiW layers and between the Ni and Ta layers were determined above 500 °C and 400 °C annealing, respectively. The Ta layer in the Ta-based barrier exhibits a stress relaxation after 500 °C annealing.

5.3 Microscopic and quantitative analyses

The TEM analysis was performed in order to determine the impact of a high temperature annealing to the barriers both microscopically and quantitatively, in addition to the material diffusion into the Si substrate. The quantitative analysis included an EDX elemental mapping, an EDX line measurement, an EDX point measurement, and an EFTEM analysis. If the bright field TEM image of the barriers before annealing in Figure 4.3 is compared with the one after annealing in Figure 4.4, an alteration is observed on the Ni and adjoining TiW layer for the TiW-based barrier and on the Ni and adjoining Ta layer for Ta-based barrier. This comparison also shows that the interface between the Si substrate and adjoining Ta layer for both barriers remains sharp, which determines that material diffusion has not taken place. The same observation is also shown for the annealed barriers deposited on the poly-Si(Ge) layer.

The quantitative analysis determines that no atoms from the barriers have diffused either into the Si substrate or poly-Si(Ge) layer. Only the Ni layer has interdiffused with the adjoining layer in both annealed barriers. The interdiffusing Ni-TiW layer is inhomogeneous in respect to the concentration of diffused elements. In this layer, a high Ni concentration was determined in the TiW layer and a low concentration of the Ti and W atoms was determined in the Ni layer. Because the grain size of the TiW layer is relatively small, ~10 nm as shown in Figure 4.4(c), there will be a large space between the grains for the Ni atoms being diffused. By applying the Scherrer equation [120] on the TiW peak at $2\theta = 40.1°$ (FWHM = 0.685°) as shown in the diffractogram of the TiW-based barrier in Figure 4.1, it is determined that the TiW grain size is 11 nm, which is in close agreement with the above TEM observation. This may imply that the TiW layer has good chemical stability, which leads to the diffusion of Ti and W atoms in a low concentration. In the Ni-Ta interdiffusing layer, the Ni and Ta atoms form a solid solution by growing a stable Ni_3Ta phase. The remaining Ta layer with ~30 nm of thickness indicates that the Ni atoms were not diffused any further. Therefore, it can be concluded that the Ni_3Ta layer has a high temperature stability, which is in agreement with a published work [123].

Additionally, an EDX surface measurement was performed using the SEM method in order to determine thoroughly the material diffusion within the poly-Si(Ge) layer. Using the Ni top layer, no material diffusion is determined or observed within the whole thickness of the poly-Si(Ge) layer. It should be noted that the purpose of the application of a Au top layer was simply to show whether the barriers could have prevented a Au diffusion into the poly-Si(Ge) layer at 600 °C annealing.

5.4 Sheet resistance and adhesion changes

The 4-probe sheet resistance (R_{sh}) measurement was performed in order to determine whether the barriers remained conductive due to annealing. The threefold increase in the R_{sh} after 600 °C annealing shows that both diffusion barriers exhibit a tolerable R_{sh} increase which remains measurable or conductive. The slight decrease in R_{sh} from 200 °C to 400 °C annealing can be related to the recrystallization and the elimination of defects within the stacked layers that cause electrons to flow within the barrier with less perturbation than before annealing. By relating to TEM analysis, it may imply that the increase in R_{sh} above 500 °C annealing is only due to the interdiffusion between the Ni and the adjoining layer in both diffusion barriers. This conclusion is plausible because electrons flow favorably within a layer having a low resistivity, which is exhibited at the lowest only by the Ni layer among the stacked layers. Thus, R_{sh} of the barriers should be subjected to a mechanical or chemical alteration in the Ni layer. Because R_{sh} of the barriers is measurable after 650 °C annealing for 24 h as well as after 600 °C annealing for 168 h, and it exhibits an insignificant increase as well, it can therefore be concluded that the interdiffusing Ni-TiW and Ni_3Ta layers have high thermal stability. This conclusion is consistent with published studies [123–125].

The decrease in barrier adhesion on the substrate from excellent to sufficient adhesion after 600 °C annealing can be caused by an induced stress during annealing. However, the barriers application in the Ni-Sn TLP wafer bonding shows a relatively high bond strength after annealing even though most of the break in the Ta-based barrier has occurred due to the barrier delamination.

5.5 Improvement in the pulse-plated Ni and Sn structures

In order to deposit Ni and Sn structures on a 6"- and 8"-wafer using the electroplating method and a small amount of electrolyte, a lab-scale electroplating tool was developed. The tool has a wafer's front side contact feature and was capable of electroplating Ni and Sn structures using a pulsed current and a wafer rotation. The purpose of this pulse plating was to deposit a uniform thickness of the Ni structures and a low surface roughness of the Sn structures. The Ni and Sn structures were pulse-plated on each barrier having the Ni top layer.

The electroplating tool which was developed, was able to perform metal depositions, *i.e.*, the Ni and Sn structures, successfully either on a 6" or 8"-wafer using the "10 ms"-pulse plating method. The wafer's front side contact feature was effectively applicable in order to establish an electrical contact between the plating base on the front of the wafer and the pulsed current source. This feature is relevant to the 8"-wafer-level processing at FhG-ISiT and is utilized commonly in electroplating production tools in the microchip industry, so that preliminary electroplating investigation of a metallic deposition on an 8"-wafer can be done using this tool.

The thickness non-uniformity of the Ni structures can be achieved <10 %, which is the critical non-uniformity for a successful wafer bonding, and it can still be achieved using high current density. A deposition rate of 0.27 µm/min is relatively high and the cathode efficiency can be as high as 93.1 %, which is the range of the typical cathode efficiency of Ni electroplating [93].

The "10 ms"-pulse plating is capable of depositing the Sn structures which have a low surface roughness. The surface roughness of the interlayer, *i.e.*, the Sn layer, is very important in the TLP bonding method because if the roughness is high, then a significant formation of voids at discrete locations can be exhibited within the bond solder due to an insufficient Sn on

those locations [76]. A roughness of 0.47 µm can be achieved using a peak current of 3 A/dm^2 density for 9 min. This relatively low roughness can still be achieved for the prolonged pulse plating duration. A noticeable pulse plating is the deposition of the ~11-µm-thick Sn structure, which still has a low roughness even if high current density of "1 s"-pulse plating is applied. As compared to the previous work using the DC current [94], the Sn surface roughness achieved is an outstanding improvement in depositing Sn structure using the same electroplating tool.

5.6 Reliability investigation of the Ni-Sn TLP bond solder

The Ni-Sn TLP bond solder was fabricated using the wafer bonding technique on which the fabrication of the high temperature µTEG is based. The solder served as electrical joints between each of the TE material pairs. In respect to the high temperature application, the solder reliability was then investigated in order to determine its mechanical and electrical stability. Therefore, after wafer dicing, the bonded dies consisting of a 16×16-array of a $100 \times 100\,\mu m^2$ bond structure and of a daisy chain structure were taken to a shear test and to a 4-probe resistance measurement, respectively. These two investigations were performed before and after 600 °C annealing for 24 h. A phase change of the bond solder due to the annealing was also investigated using an EDX point measurement in the SEM method in order to analyzed the dependency of the bond time and bond pressure on the stability of the bond solder.

Before and after annealing, the bond solder exhibited a relatively high bond strength and a tolerable increase in the electrical resistance. The re-melting of the bond solder was not observed during 600 °C annealing. In contrast to the work of *Welch III* [73], the Ni-Sn TLP wafer bonding can be performed using 15 min bond time instead of 60 min because both bond times resulted in a similar Ni-Sn phase within the bond solder. The variation in bond pressure could not create a thick Ni-Sn IMC which could prevent voids formation after annealing. However, the formation of voids can be overcome by creating a Ni-Sn bond solder structure surrounded by a Ni-Sn IMC layer as will be discussed in Section 5.6.3. The optimal thickness of the Ni and Sn layer is shown by wb-E (3.4 µm and 2.9 µm for the Ni and Sn layer, respectively) because the resulting bond solder exhibits the lowest electrical resistance after annealing among the investigated wafer bonding. In addition, the thickness of both layers is sufficient, taking the daisy chain structure into account, for growing a Ni-Sn bond solder which has significantly fewer void formations.

5.6.1 Ni-Sn phase transformation

Before annealing, the Ni-Sn TLP bond solder contains mainly a Ni_3Sn_4 phase and may contain a Ni_3Sn_2 phase as well. Because the growing layer within the bond solder shows a homogeneous visual appearance either in the optical microscope images or in the SEM images, the whole thickness of the growing layer is determined that it contains a homogeneous Ni_3Sn_4 phase. Wafer bonding using different bond times and bond pressures results in a similar microstructure of the bond solder. Hence, the material homogeneity of the bond solder does not depend neither on the bond time nor on the bond pressure. Furthermore, the 60 min of bond time cannot create a homogeneous phase of the bond solder because all molten Sn is already consumed in growing the stable Ni_3Sn_4 phase. If the Sn layer is deposited thickly enough in order to grow a homogeneous phase within the bond solder, then the molten Sn can overflow during wafer bonding under the applied bond pressure. Such an overflow is undesirable in a microchip

application because it can create a short-circuit problem between the functional microstructures [126]. After 600 °C annealing, the Ni_3Sn_4 phase transforms to the Ni_3Sn phase followed by a significant void formation within the layer of this new phase. During this transformation, three Sn atoms from a Ni_3Sn_4 molecule diffuse further into the unconsumed Ni layer, so that the unconsumed Ni layer becomes thinner than before annealing. The significant void formation could be due to the molecular structure difference, in which the lattice parameter of the Ni_3Sn phase (close-packed structure [127], $a = b = 5.275$ Å, $c = 4.234$ Å [128]) is smaller than the Ni_3Sn_4 phase ($a = 12.214$ Å, $b = 4.060$ Å, $c = 5.219$ Å [129]), and due to the density difference, which the Ni_3Sn phase ($\rho = 9.37$ g/cm^3 [127]) is denser than the Ni_3Sn_4 phase ($\rho = 8.62$ g/cm^3 [130]). Therefore, the Ni-Sn IMC layer "shrinks" during annealing, thus leaving empty spaces (voids). The Ni_3Sn_2 phase formation on both sides of the bond solder cross-section (left and right sides in Figure 4.22-*bottom*) is due to the interdiffusion between the Ni and Sn layers, which are not consumed after wafer bonding at the edges of the bond solder (left and right sides in Figure 4.22-*top*). This interdiffusion is so strong that the unconsumed Ni layer's edges become thinner. The formation of the Ni_3Sn_2 phase instead of the Ni_3Sn phase has an unclear mechanism. However, it seems that the Ni_3Sn_2 phase grows preferably in a layer next to the surface as also observed in Figure 5.1. The re-melting of the bond solder did not occurred during 600 °C annealing because the displacement or the detachment of the top substrate of a bonded die was not observed as the top substrate serves as the foothold during annealing. This observation is evidence that the re-melting temperatures of the three Ni-Sn phases are above 600 °C as stated in the Ni-Sn phase diagram.

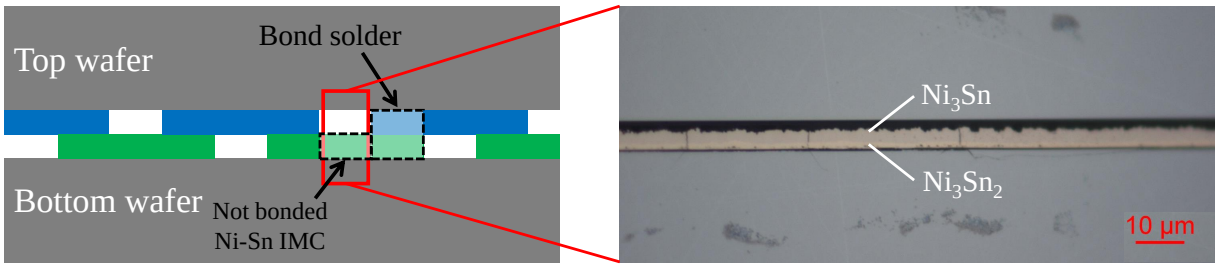


Figure 5.1: Cross-sectional sketch of a daisy chain structure (*left*, blue and green structures corresponds to the electroplated Ni and Sn layers on the top and bottom wafers, respectively). Cross-sectional microscope image of a not-bonded part of the daisy chain structure (*right*, the representation of red square in the left sketch) after annealing. The determined phases are based on the EDX analysis that the Ni_3Sn_2 phase is always observed as a top layer.

5.6.2 Mechanical stability of the bond solder

The bond solder was fabricated on each barrier which has the Ni top layer. All of the fabricated bond solder exhibit a higher bond strength than the minimum required bond strength based on the MIL-STD-883G (Method 2019.7) standard after fabrication. The break distribution analysis also show that no delamination encountered on the Ni top layer. This demonstrates that the Ni top layer can be effectively applied as a plating base for depositing the Ni and Sn structures.

The bond solder, which was fabricated in wb-A and wb-B (both using 60 min of bond time), exhibits lower bond strength than the other fabrications (wb-C - wb-H). However, this is not due to the long duration of wafer bonding but rather due to the formation of voids in wb-A and the substrate mechanical stability in wb-B. The more voids are formed, the more break within bond solder occurs. In addition, the bond strength is also influenced by a significant misalignment

between the top and bottom wafers as occurred in wb-C. The more significant the misalignment is, the lower the bond strength is determined. The increase in the bond strength after annealing indicates that the Ni_3Sn and Ni_3Sn_2 phases have higher mechanical stability than the Ni_3Sn_4 phase.

5.6.3 Electrical stability of the bond solder

The daisy chain structure has a part where the pulse-plated Ni and Sn structures are not bonded but they create a Ni-Sn IMC layer as depicted in Figure 5.2. During annealing, Sn atoms may be diffused from this part into the bond solder because the pulse-plated Ni layers within the bond solder is still available after the growth of the Ni_3Sn layer. This diffusion fills the voids, which are formed within the Ni_3Sn layer. Therefore, the daisy chain bond solder exhibits an insignificant void formation after annealing as depicted in Figure 4.23-*top*. If the Ni layer is electroplated too thinly, then the unconsumed Ni layer after annealing will become thinner and after a certain time the Sn atoms will not diffuse further because the Ni structure is completely consumed as depicted in Figure 4.21-*bottom*.

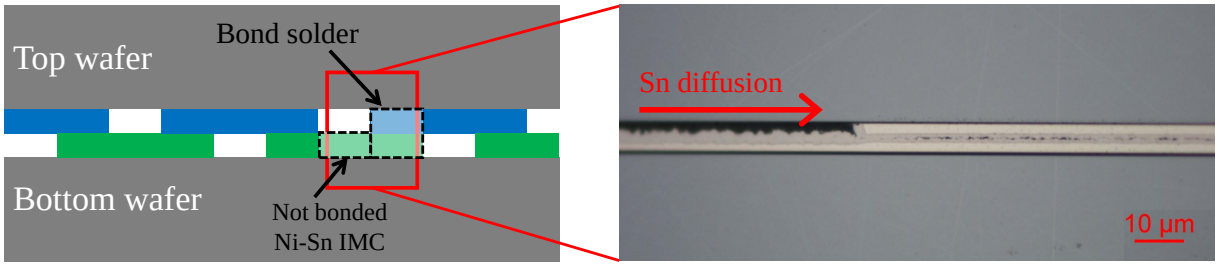


Figure 5.2: Cross-sectional sketch of a daisy chain structure (*left*, blue and green structures corresponds to the electroplated Ni and Sn layers on the top and bottom wafers, respectively). Cross-sectional microscope image of a bond solder with its not-bonded part within the daisy chain structure (*right*, the representation of red square in the left sketch) before annealing.

Based on the discussion above, the increase of the daisy chain resistance is not mainly due to the void formation within the bond solder but rather due to the incorporated layers in the daisy chain structure. Before annealing, the daisy chain resistance depends on the thickness of the unconsumed Ni layers as shown in Figure 4.27-*left*. This is obvious because the unconsumed Ni layer is available in all parts of the daisy chain structures, thus a charge carrier transport takes place preferably within the unconsumed Ni layer. However, this dependency is disturbed after annealing because the unconsumed Ni layer in the not-bonded part of the daisy chain structure is completely consumed producing the Ni_3Sn_2 and Ni_3Sn phases. Hence, the determinant factor in varying electrical resistance of the daisy chain after annealing is the not-bonded part of the daisy chain structure because in this part, the charge carrier transport takes place within a longest line in contrast to the charge carrier transport, which takes place across the bond solder. Consequently, the Ni_3Sn_2 and Ni_3Sn phases within the not-bonded part of the daisy chain structure are responsible for increasing the daisy chain's electrical resistance. In Figure 4.24-*right*, wb-C exhibits a high daisy chain resistance because there is a significant formation of voids within the bond solder after annealing as shown in Figure 4.23-*bottom*. This significant formation of voids results from the thin electroplated Ni layer (1.7 µm of thickness, see Table 3.3) in wb-C.

The charge carrier transport within the daisy chain structure is analogous to a charge carrier transport within a μTEG. If the bond solder, *i.e.*, the joint between TE material structures, exhibits high resistance due to a significant void formation, then the charge carrier transport, which takes place from a *p*-type TE material structure to a *n*-type TE material structure and so forth, can be perturbed. Since this can lead to the degradation of μTEG performance, therefore, it is preferable to fabricate a bond solder without the void formation. The design of a bond solder structure which will exhibit a significantly low void formation can be considered and proposed from the daisy chain structure. As sketched in Figure 5.3, a bond solder structure can be surrounded by the Ni-Sn IMC layer, which will be the resource of Sn atoms which will diffuse into bond solder during annealing, thus the void formation can be prevented. This bond solder structure should be accompanied with a sufficient thickness of the electroplated Ni structure.

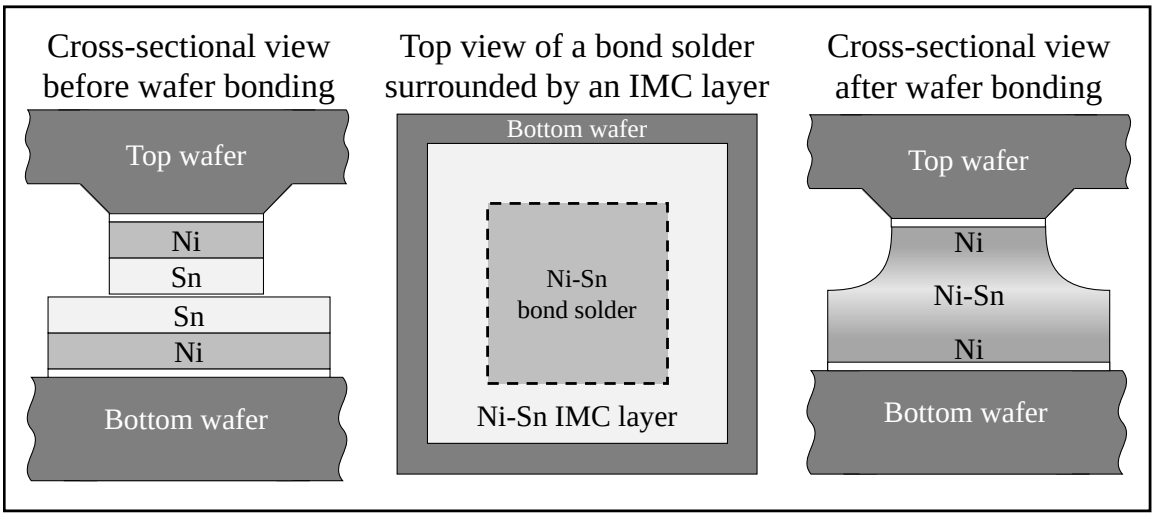


Figure 5.3: Sketch of an improved bond structure design.

5.7 Contact resistivity change due to annealing

A so-called TLM structures were fabricated using surface micromachining in order to determine the contact resistivity ρ_C between each barrier and poly-Si layer. For this investigation, both barriers with and without the Au top layer were fabricated, each on a wafer. The impact of annealing on the ρ_C stability was also investigated. Additionally, the material diffusion can also be determined by investigating the impact of annealing on the sheet resistance R_{sh} of the poly-Si layer. The investigation determines that ρ_C and R_{sh} are stable up to 500 °C.

A significant change in R_{sh} of the poly-Si layer and in ρ_C between the barrier and the poly-Si layer after 600 °C annealing is due to the Au diffusion, which is evident from the TEM analysis. The result of R_{sh} and ρ_C from TLM structure with G10 of gap type can be neglected because the values are scattered greatly due to the fabrication sensitivity. In order to determine R_{sh} and ρ_C after 600 °C annealing, TLM structures without the TLM Au pads were fabricated and then measured manually. The change of R_{sh} as well as ρ_C without the TLM Au pads from 300 °C to 500 °C of annealing is in accordance with the change of both parameters for both barriers which have the TLM Au pads. At 600 °C of annealing, both parameters increase although no material diffusion into the poly-Si layer takes place. This increase could be due to the poly-Si layer stress induced by the presence of the barrier, the interdiffusion between the Ni and the TiW

layers, and the growth of the Ni_3Ta phase. The decrease of R_{sh} and ρ_C for the TiW-based barrier after 650 °C annealing can be assumed that materials from the TiW-based barrier diffuse into the poly-Si layer, so that the mixture between the metallic material and Si creates a compound with a low resistivity. For the Ta-based barrier, the growth of the α-Ta phase within the Ta layers and the stress relaxation of the Ta layer adjoined to the Si substrate is assumed to be responsible for increasing both parameters significantly after 650 °C annealing.

Since ρ_C between each barriers and poly-Si layer is relatively stable up to 500 °C annealing, a poly-Si-based μTEG consisting of TiW-based or Ta-based barrier can effectively work in converting a 500 °C heat without decreasing its performance. The increase of ρ_C at 600 °C annealing may disturb the μTEG performance. However, the material's figure of merit of the poly-Si or poly-SiGe layer will not deteriorate because both barriers are capable of preventing material diffusion into both layers as evidenced in the TEM analysis, so that the μTEG can still work in converting heat into electrical power.

Chapter 6

Summary and recommendation

6.1 Summary

Electrical power can be generated from heat by using a TEG. In microsystem technology, a micro-scale TEG (μTEG) can convert high temperature heat up to 600 °C into power by integrating a poly-SiGe material as a TE material. The poly-SiGe material enables heat-to-power conversion at high temperature because it has a figure of merit ranges from temperature of 400 °C to 1000 °C. In a μTEG fabrication, a wafer bonding technique may be applied to join *p*-type and *n*-type poly-SiGe structures using a bond solder so that a thermopile device can be created. In order to prepare the bond solder, layers/structures for solder components are commonly deposited using an electroplating method on a wafer pair. This method requires a plating base where structures of the solder components are deposited. In respect to high temperature applications, the joint, *i.e.*, the bond solder and the plating base, must be thermally stable, *i.e.*, the must remain mechanically strong and electrically conductive, and prevent material diffusion (diffusion barrier) into the poly-SiGe structures. To the best of the author's knowledge, the applications and the developments of a μTEG for high temperature applications have not been commercialized or published so far. A possible reason for this is that a high thermally stable joint between the TE materials has not yet been developed.

The objective of this study is first to develop a diffusion barrier as well as a bond solder which are thermally stable and reliable for high temperature applications so that they can be integrated to a μTEG operated at 600 °C. For the diffusion barrier, two types (TiW-based and Ta-based) barrier have been intensively investigated using an XRD analysis, a TEM analysis (EDX and EFTEM analyses), a 4-probe sheet resistance measurement, and an adhesive tape test. These methods were performed before and after 600 °C annealing for 24 h in order to investigate the barrier's stability. The contact resistivity between each barrier and a poly-Si layer has been determined and investigated before and after annealing. For the bond solder, a so-called Transient Liquid-Phase (TLP) wafer bonding technique was developed in order to fabricate a highly mechanically and electrically stable bond solder. The bond solder components were made from an intermetallic compound between Ni and Sn layers (Ni-Sn IMC). The chemical composition of the Ni-Sn IMC as well as the mechanical and electrical stability of the Ni-Sn TLP bond solder have been intensively investigated before and after annealing. The mechanical investigation was performed using a shear test method an a break distribution analysis on bonded dies, which consist of a 16×16-array of a $100 \times 100\,\mu m^2$ bond structure. The electrical investigation was performed using a 4-probe electrical resistance measurement on bonded dies, consisting of a daisy chain structure.

The main results of the study presented here and their implications for the high temperature μTEG are as follows:

– Both diffusion barriers which have been developed can prevent material diffusion into the poly-Si or poly-SiGe layers at 600 °C annealing. Therefore, the figure of merit for the TE material, which is made from the poly-SiGe structures, will not deteriorate during heat-to-power conversion.

– Using a 100 -nm-thick Ni top layer, the contact resistivity between each diffusion barrier and the poly-Si layer is stable up to 500 °C annealing. This stability will ensure that the poly-SiGe-based μTEG will operate optimally up to 500 °C. The increase in contact resistivity at 600 °C annealing may reduce the optimal performance of the μTEG, however, as pointed out in the previous main result, the μTEG can still work flawlessly because material diffusion into the TE material has not occurred at this temperature.

– A lab-scale electroplating tool, which is equipped with a wafer's front side contact feature, has been developed for the adaptability of the 8"-wafer-level processing between FhG-ISiT and CAU Kiel. The tool utilizes a pulse plating method and a wafer rotation feature to deposit Ni and Sn structures, which have a high thickness uniformity and a low surface roughness, respectively. This deposition has been successfully performed both on a 6"- and 8"-wafer using a plating base which consists of each of developed barrier with the 100 -nm-thick Ni layer.

– After 600 °C annealing, the Ni-Sn TLP bond solder exhibits a relatively high bond strength and a tolerable electrical increase. From this result, the adhesion of both barriers on the substrate has also remained strong. Thus, a μTEG, which consists of the diffusion barriers and the Ni-Sn TLP bond solder, will work with a good mechanical and electrical stability.

The significant results of the development of the barrier are as follows:

– The barriers were fabricated in a form of stacked thin films where the TiN barrier was sandwiched with TiW barriers and Ta barriers for the TiW-based and Ta-based barriers, respectively. By fabricating such stacked thin films, the barrier can exhibit a low tensile stress so that a wafer curvature can be significantly reduced. For the Ta-based barrier, sandwiching of the TiN barrier can be advantageous because the TiN layer is thermodynamically stable against a TaN formation. Due to the good chemical stability of the TiW barrier, it is assumed that nitrogen will not diffuse from the TiN barrier into the sandwiching TiW barrier.

– Using a Ni layer as the top layer on both barriers, no phases of compounds between Si and Ni atoms or between Si and barrier's elements (silicides) after 600 °C annealing are grown whether the barriers are deposited on a single crystalline substrate or on a poly-Si(Ge) layer. This indicates that no material diffusion into the substrate has taken place during annealing. The TEM investigation supports this result and gives microscopic and quantitative details.

– Both barriers exhibited a tolerable sheet resistance increase after 600 °C annealing and their adhesion to the Si substrate is not degraded.

– Contact resistivity between each barrier and the poly-Si layer is determined and relatively stable up to 500 °C annealing. As the best barrier, the TiW-based barrier can be chosen because it exhibits a low contact resistivity increase on the poly-Si layer after 600 °C annealing.

The significant results of the development of the bond solder are as follows:

– A lab-scale electroplating tool was successfully employed to electroplate Ni and Sn structures on a 6"- or an 8"-wafer. Using a pulsed current, the Ni structures and subsequently the Sn structures can be electroplated on the wafer which has a plating base, and which consists of the developed barrier and the Ni top layer. With this pulse plating method and a wafer rotation, the thickness non-uniformity of the Ni structures and the surface roughness of the Sn structures can be improved significantly below 10 % and below 0.5 µm, respectively, over the wafer surface. The deposition rate can also be increased without reducing the thickness uniformity and increasing the surface roughness.

– The TLP wafer bonding was successfully performed to fabricate the Ni-Sn bond solder for a short bond time at a bond temperature of 300 °C. After wafer bonding, the Ni-Sn IMC of the bond solder contains mainly a Ni_3Sn_4 phase. After 600 °C annealing, this phase is transformed into a Ni_3Sn phase creating a denser IMC layer together with a voids formation. Based on the daisy chain structure, a design (see Figure 5.3) of a bond solder structure for joining the TE materials is proposed so that a voids formation within the bond solder can be significantly reduced. Moreover, no re-melting of the bond solder is observed.

– The Ni-Sn bond solder exhibits a relatively high bond strength as well as a tolerable electrical resistance increase of the daisy chain structures before as well as after 600 °C annealing. The high bond strength indicates also that the TiW-based and Ta-based barriers with the Ni top layer exhibit an excellent adhesion to the substrate. The resistance increase of the daisy chain structures is not mainly due to the Ni-Sn phase transformation within bond solder but rather due to a part of the daisy chain structure which is not bonded. The required thickness of the Ni and Sn structures is approx. 3.4 µm and 2.9 µm, respectively, in order to fabricate a Ni-Sn bond solder which exhibits a highest bond strength and a lowest electrical resistance after 600 °C annealing.

6.2 Recommendation

From this work, some recommendations are given in order to improve the stability of diffusion barriers, the Ni-Sn TLP wafer bonding, and the contact resistivity between the barriers and poly-Si layer for high temperature application up to 600 °C.

– After vacuum breaks in the barrier deposition, pre-etching of native oxides on the wafer should always be performed before a subsequent thin film deposition in order to enhance the adhesion of the barriers to the substrate as well as to reduce significantly the influencing factors at the interface between the barriers and poly-Si layer.

– In the Ta-based barrier, the Ta layer, which is adjoined to the substrate, can be deposited thinner than 100 nm, for example 20 nm, in order to significantly minimize the induced stress relaxation within the Ta layer during annealing.

– An improved bond structure design as illustrated in Figure 5.3, which accommodate Ni-Sn TLP bond solder surrounded by the Ni-Sn IMC layer, can be created. With this design, the voids formation within the Ni-Sn bond solder can be reduced significantly during the Ni-Sn phase transformation during 600 °C annealing. This bond solder structure should be accompanied with a sufficiently thick electroplated Ni structure.

Appendix

A Supplementary information

A.1 EDX profiles subtraction to obtain the Si EDX profile

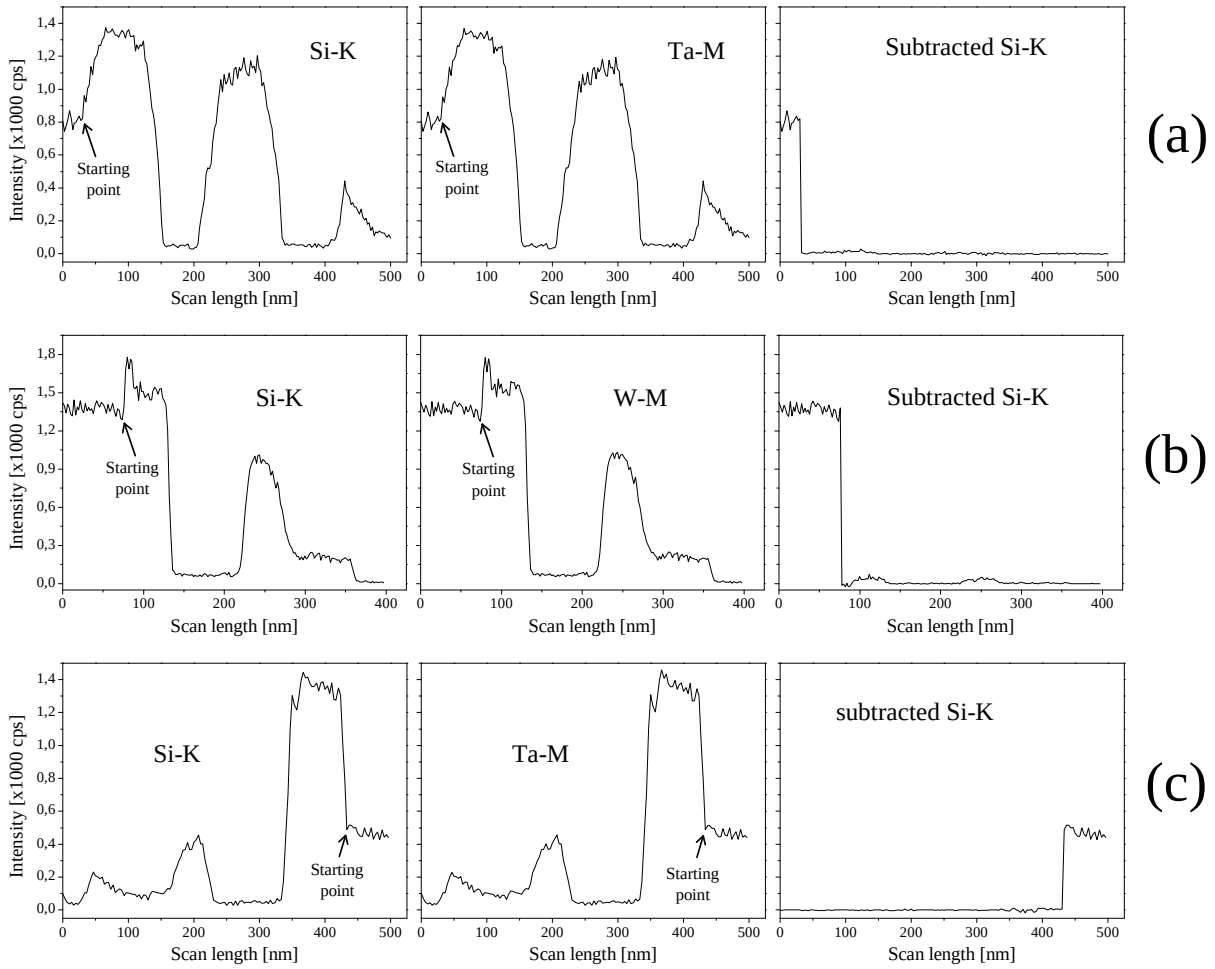


Figure A.1: Subtraction of the Si-K EDX profile with the W-M and Ta-M EDX profiles for both barriers deposited on the *c*-Si substrate: (a) the Ta-based barrier before annealing, (b) the TiW-based after annealing, (c) the Ta-based barrier after annealing, (d) the TiW-based deposited on the poly-Si layer after annealing, (e) the Ta-based barrier deposited on the poly-SiGe layer after annealing, (f) the TiW-based barrier with Au top layer after annealing, and (g) the Ta-based barrier with Au top layer after annealing.

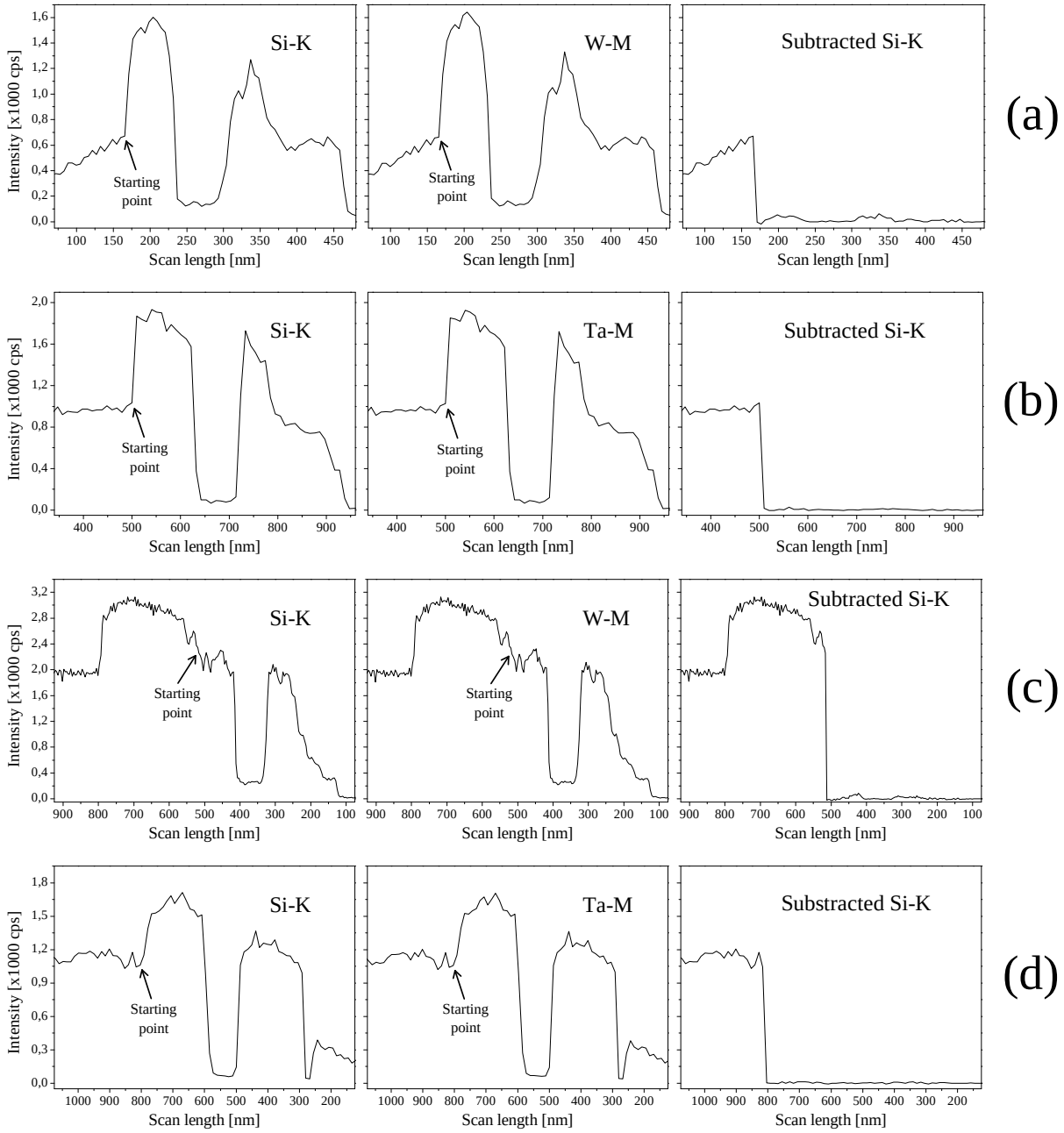


Figure A.2: Subtraction of the Si-K EDX profile with the W-M and Ta-M EDX profiles for both barriers deposited on the poly-Si layer: (a) the TiW-based barrier deposited on the poly-Si layer after annealing, (b) the Ta-based barrier deposited on the poly-SiGe layer after annealing, (c) the TiW-based with Au top layer deposited on the poly-Si layer after annealing, and (d) the Ta-based with Au top layer deposited on the poly-SiGe layer after annealing.

A.2 Energy spectra analyses

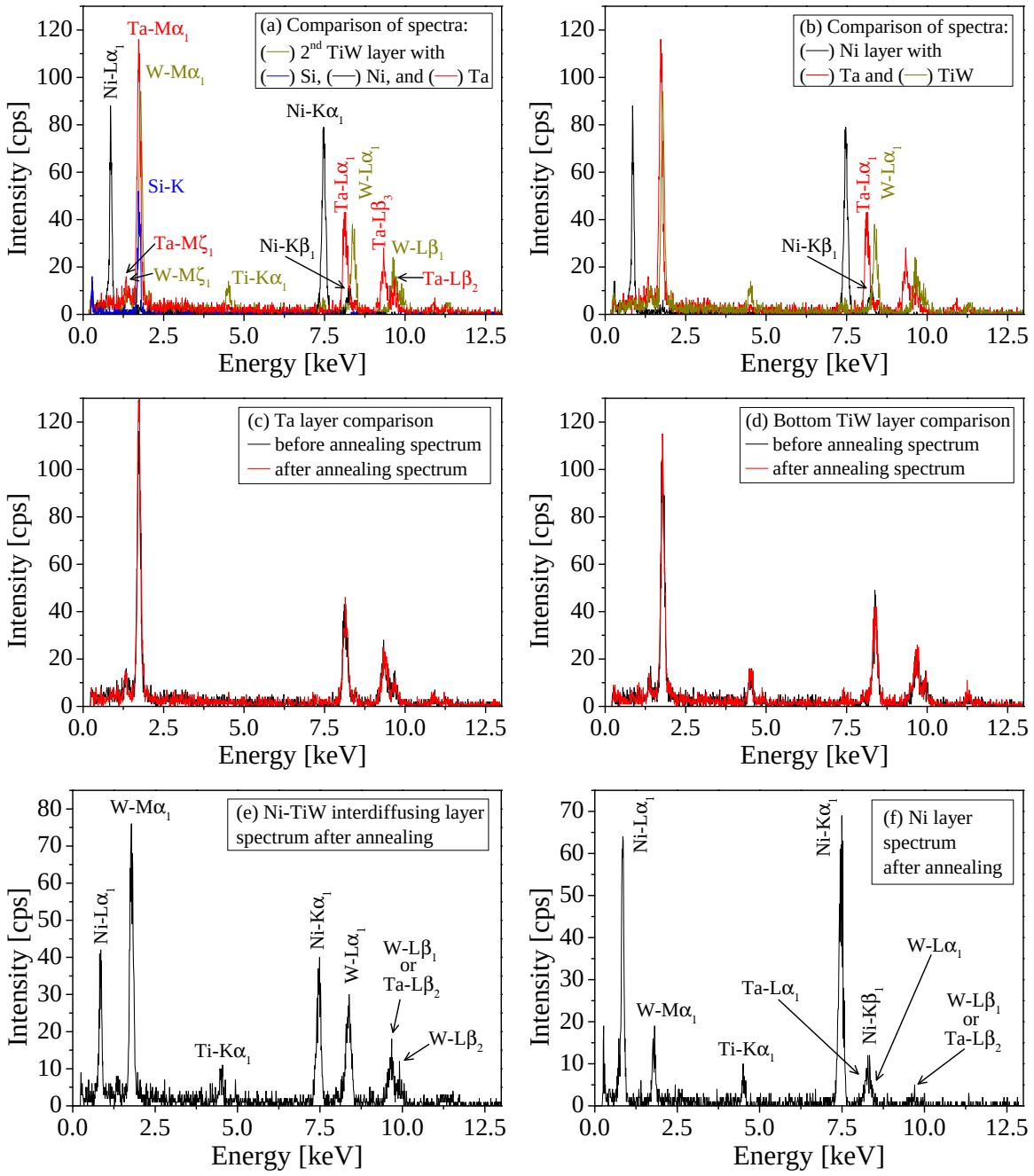


Figure A.3: Energy spectra analyses to determine the overlapping EDX profiles in the TiW-based barrier: (a) on the TiW layer adjoined to the Ni layer before annealing, (b) on the Ni layer before annealing, (c) on the Ta layer before and after annealing (similar spectra), (d) on the TiW layer adjoined to the Ta layer before and after annealing (similar spectra), (e) on the interdiffusing Ni-TiW layer (the Ta-L profile appears in this layer because Ta-Lβ_2 is adjacent to W-Lβ_1), and (f) on the Ni layer after annealing (the Ta-L profile appears in this layer because Ta-Lα_1 and Ta-Lβ_2 are adjacent to W-Lα_1 and W-Lβ_1, respectively).

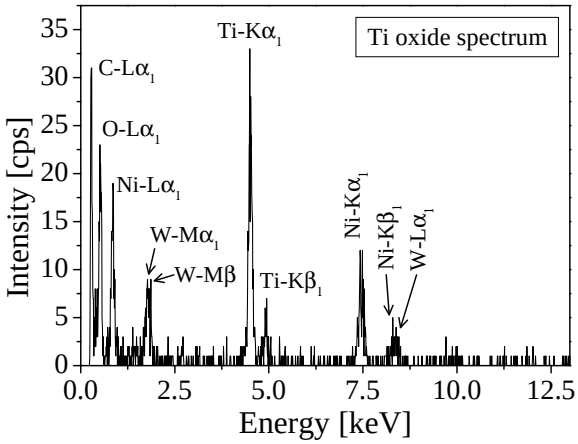


Figure A.4: Energy spectra on the surface of the Ni layer where the Ti oxide grown after annealing for the TiW-based barrier.

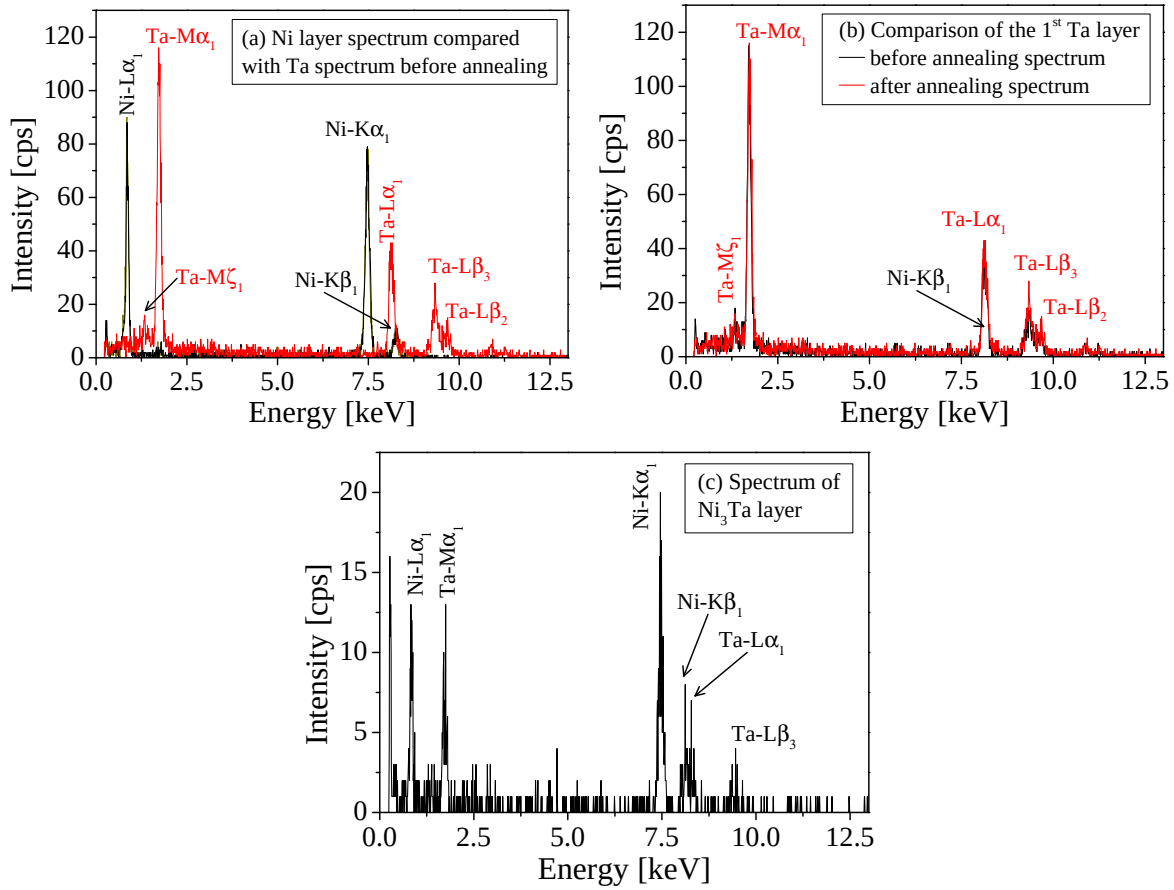


Figure A.5: Energy spectra analyses to determine the overlapping EDX profiles for the Ta-based barrier: (a) on Ni layer before annealing (the Ta-L profile appears in this layer because Ta-Lα_1 is adjacent to Ni-Kβ_1, (b) on the Ta layer adjoined to the *c*-Si substrate before and after annealing (similar spectra), and (c) on the Ni_3Ta layer.

A.3 TEM micrographs on both Au-top-layered diffusion barriers deposited on the poly-Si and poly-SiGe layers after annealing

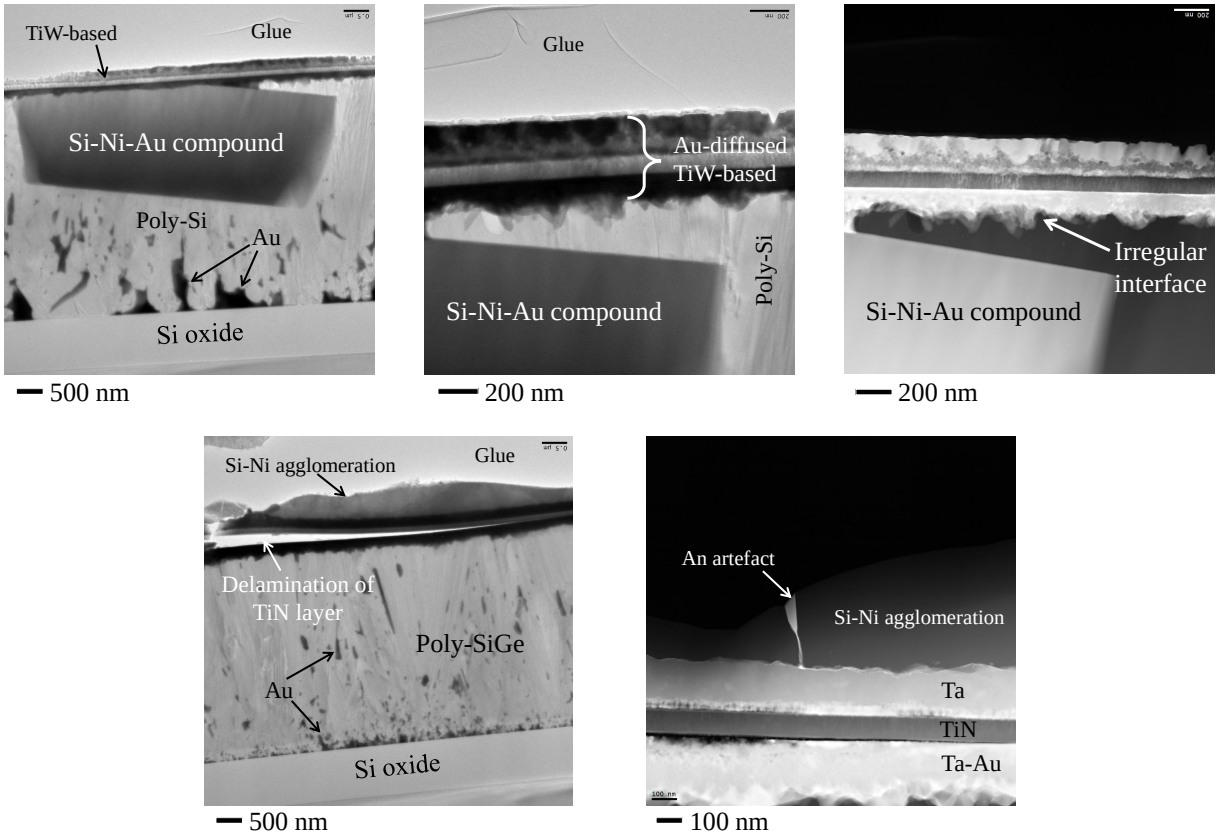


Figure A.6: TEM micrographs for the annealed TiW-based (*top*) and Ta-based (*bottom*) barriers, where the Au diffusion and some interesting artifacts are observed.

A.4 SEM micrographs of the TLP bond solder

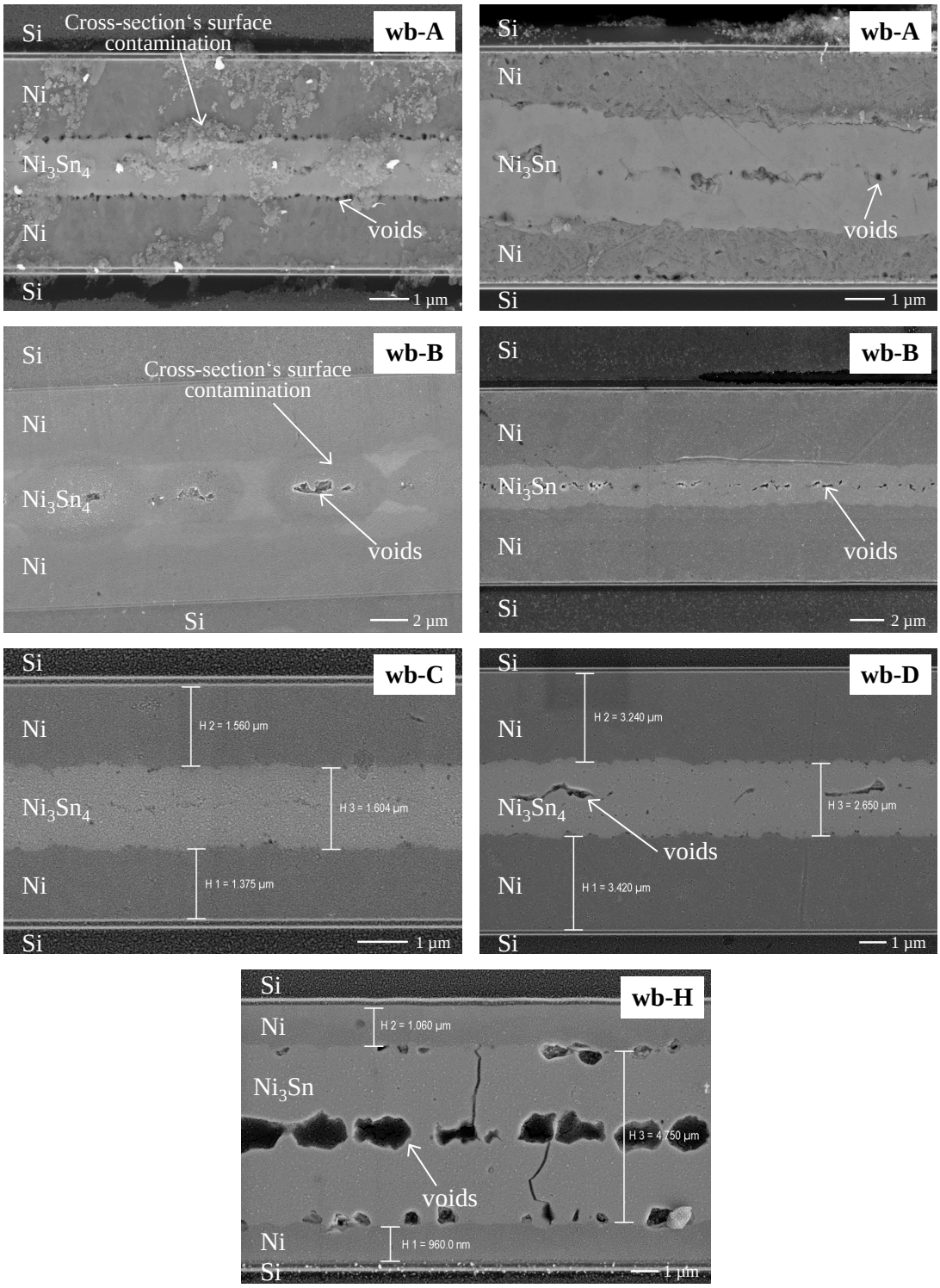


Figure A.7: SEM micrographs of the TLP bond solder: wb-A and wb-B before (*left*) and after (*right*) annealing, wb-C and wb-D before annealing, and wb-H after annealing.

A.5 TLM measurement using an electroplated Au layer as the TLM pads

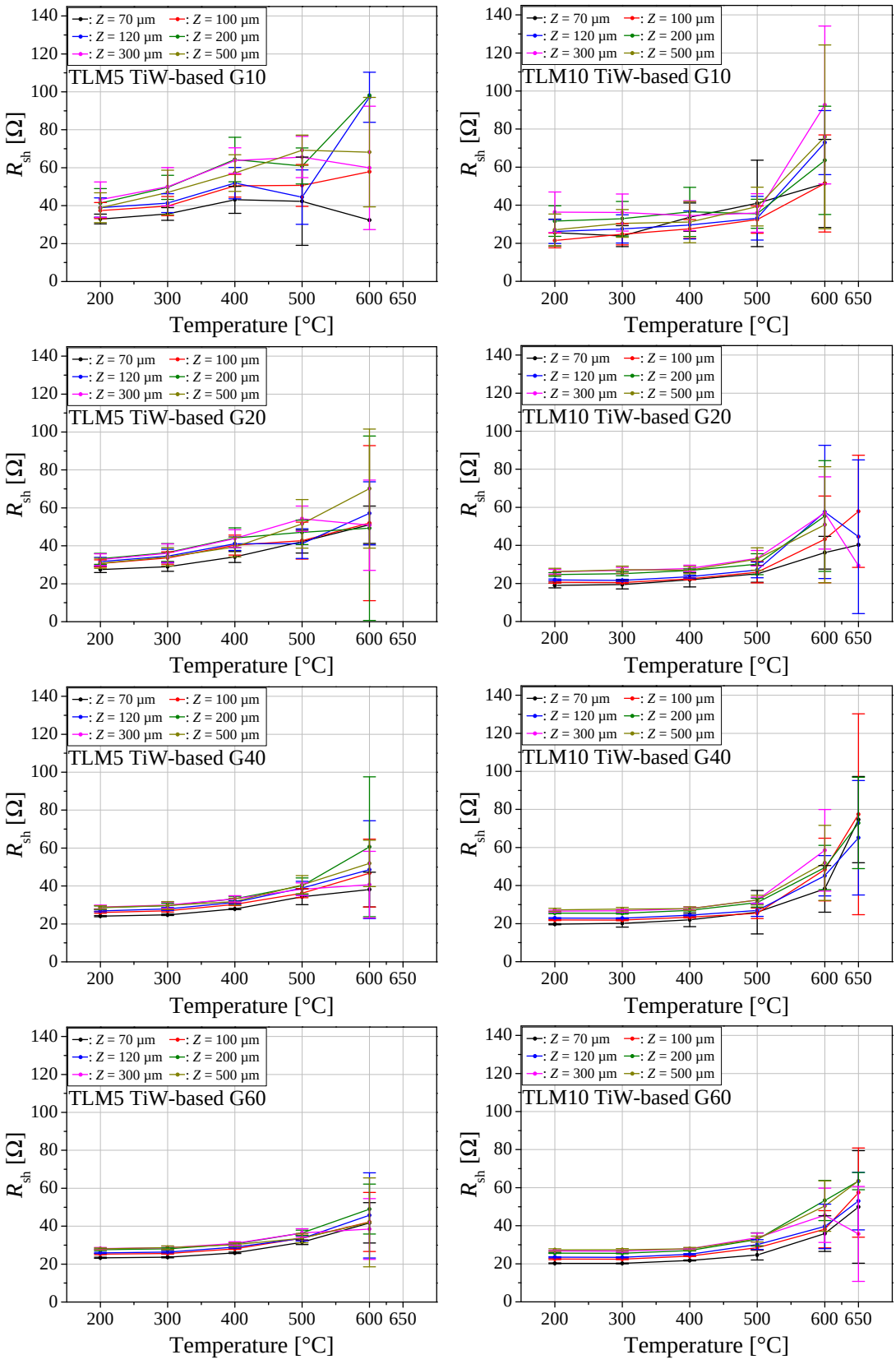


Figure A.8: Sheet resistance R_{sh} of the TiW-based barrier for TLM5 (*left*) and TLM10 (*right*).

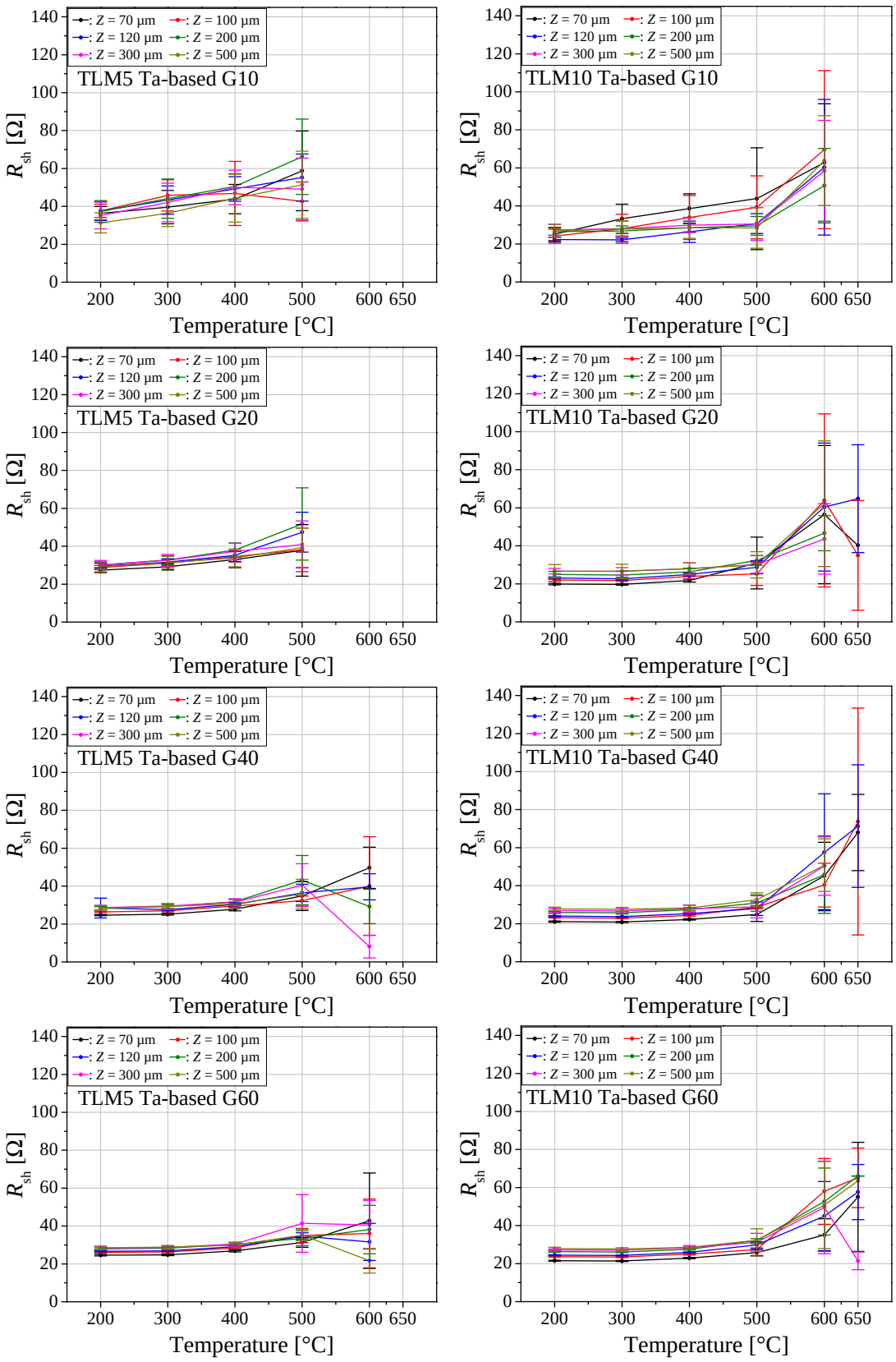


Figure A.9: Sheet resistance R_{sh} of the annealed Ta-based barrier for TLM5 (*left*) and TLM10 (*right*).

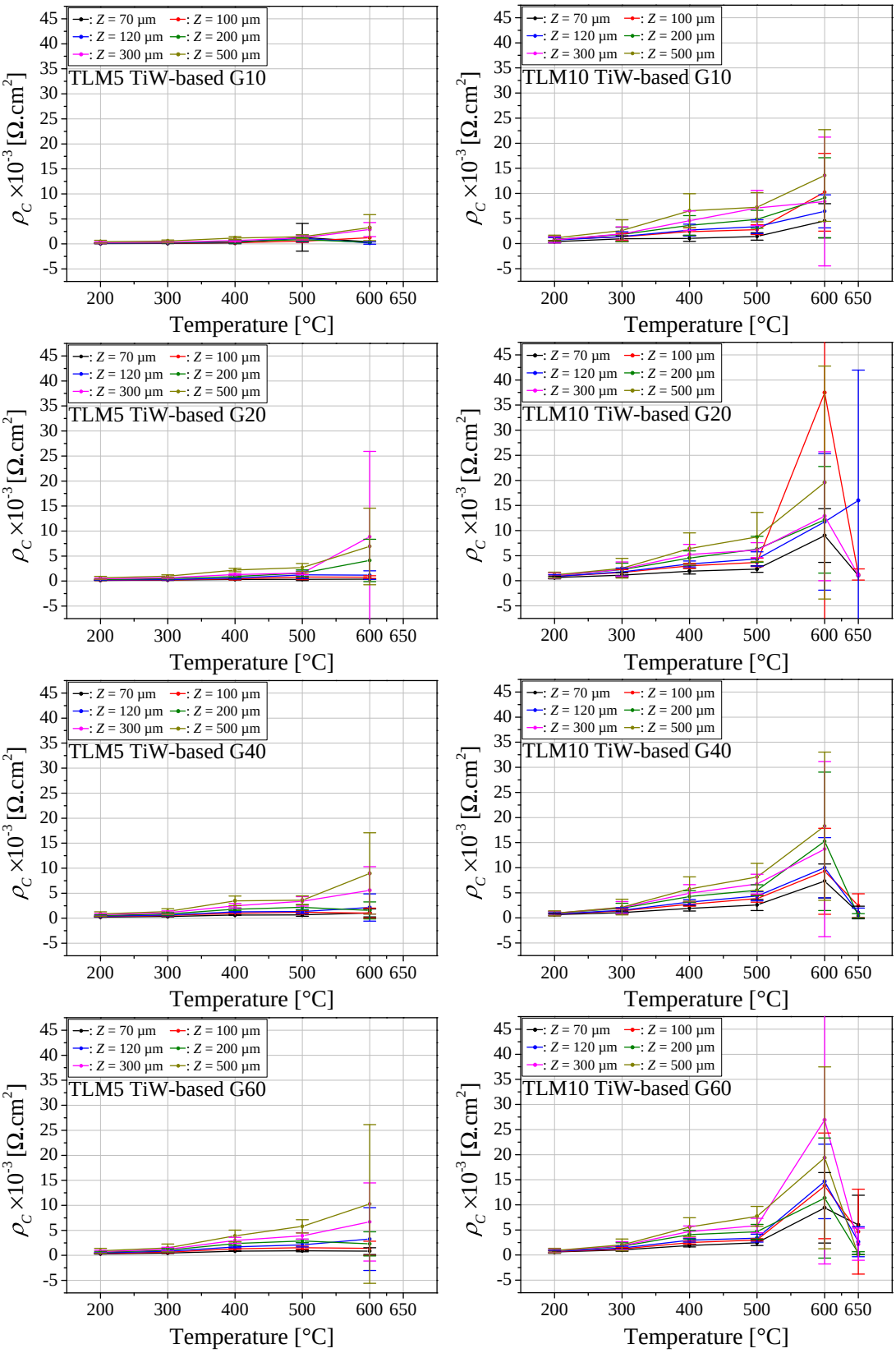


Figure A.10: Contact resistivity ρ_C of the annealed TiW-based barrier for TLM5 (*left*) and TLM10 (*right*).

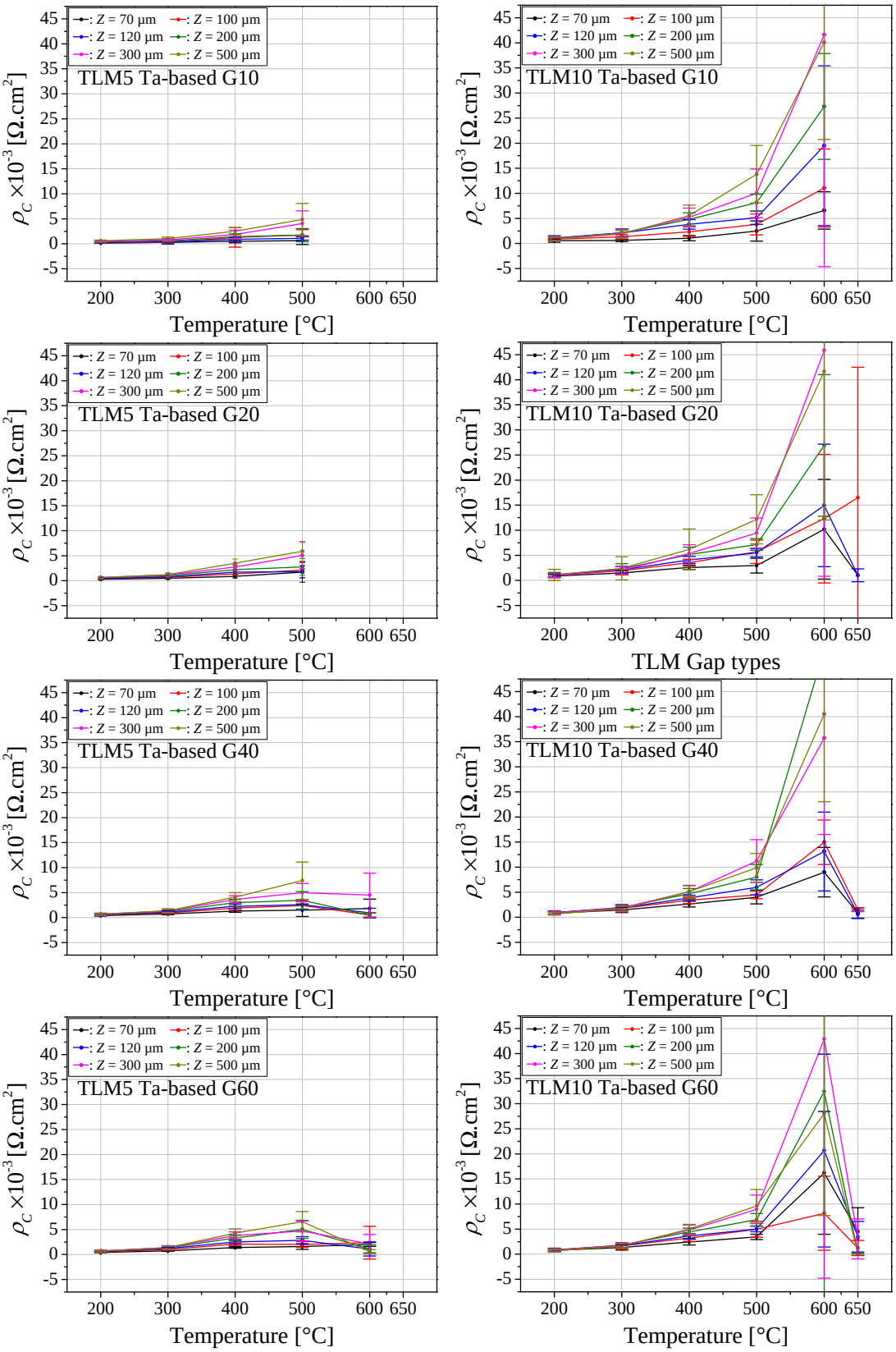


Figure A.11: Contact resistivity ρ_C of the annealed Ta-based barrier for TLM5 (*left*) and TLM10 (*right*).

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C Publications

Proceeding

BUDHIMAN, N.; SCHÜRMANN, U.; JENSEN, B.; CHEMNITZ, S.; KIENLE, L.; WAGNER, B.: High Temperature Reliability of Ta-Based and TiW-Based Diffusion Barriers. In: *Physics, of Springer Proceedings* 164 (2015), 169-174. http://link.springer.com/chapter/10.1007/978-3-319-16919-4_22

Article - accepted on 23 November 2015

BUDHIMAN, N.; SCHÜRMANN, U.; JENSEN, B.; CHEMNITZ, S.; KIENLE, L.; WAGNER, B.: Transmission electron microscopy study for investigating high temperature reliability of $Ti_{10}W_{90}$-based and Ta-based diffusion barriers up to 600 °C. In: *physica status solidi (a) - applications and materials science*. http://onlinelibrary.wiley.com/doi/10.1002/pssa.201532654/abstract

Article - accepted on 19 November 2015

BUDHIMAN, N.; JENSEN, B.; CHEMNITZ, S.; WAGNER, B.: High temperature investigation on a nickel-tin transient liquid-phase wafer bonding up to 600 °C. In: *Journal of Microsystem Technologies*. http://link.springer.com/article/10.1007/s00542-015-2738-6

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E Declaration Of Authorship

I, **Nando Budhiman**,

declare that this Ph.D. Thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

Development of high temperature diffusion barriers and transient liquid-phase wafer bonding for thermoelectric MEMS harvester

I confirm that:

1. This work was done wholly or mainly while in candidature for a doctorate degree (Dr.-Ing.) at Christian-Albrechts-University of Kiel, Germany;

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5. I have acknowledged all main sources of help;

6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

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